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Case Studies in Surface Analysis of Electronic Materials

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Most of electronic devices consist of multilayer systems formed from semiconductors, metals, and insulators. The thickness of layers is becoming very thin. For a typical example, the thickness of a gate oxide layer is less than about 10 nm in an MOS (metal-oxide-semiconductor) device. Therefore, the role of surfaces and/or interfaces is very important in the recent electronic technology. This trend also means that an evaluation method of surfaces and interfaces is valuable and a new technology of surface characterization is required to fabricate a small size device with high performance.

Several interesting results are presented, which have been investigated in NTT laboratories using surface analysis techniques.

1) Roughness estimation of thermally oxidized silicon surfaces using AFM

A silicon surface is composed from atomically flat terraces and atomic steps when it is heated up and cleaned in UHV. On the other hand, it is reported that the surface roughness on the order of sub-nm of a silicon oxide layer affects the electronic characteristics. Using AFM, we have investigated the roughness of silicon surfaces thermally oxidized at various temperatures. It is found that the roughness decreases with increasing the oxidation temperature.

2) Removal of oxide layers on GaAs surfaces by de-ionized water using XPS

The removal technique for oxide layers has been investigated on GaAs substrates using de-oxygenated de-ionized water. The chemically treated samples were transferred to an XPS apparatus without atmospheric exposure. It is found that oxide layers are easy to be removed when samples are dipped for appropriate time in water in which the dissolved oxygen concentration is low. For the case of long-time dipping, it is also found that the enrichment of the arsenic concentration takes place at the surface.

3) Thermal behavior of thin silicon layer on silicon oxide using AES

The thermal migration of silicon atoms has been investigated for thin silicon layers on silicon oxide layers buried in silicon substrates. When the sample was annealed at 1100°C, hexagonal faceted holes were formed in an overlayer silicon layer. The diagonal of holes was about 1 μm and the atomic components of silicon oxide were two-dimensionally observed through holes by AES. When the sample was annealed at 1200°C, silicon atoms agglomerated and formed islands of about 0.1 μm in diameter on a silicon oxide layer.

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