Proceedings of the 11th
KACC, October 1996

DC VOLTAGE CONTROL BY DRIVE SIGNAL PULSE-WIDTH CONTROL OF FULL-BRIDGED INVERTER

°Junichi ishikawa*, Taiju Suzuki*, Hiroaki Ikeda*, Yoko Mizutani*, Hirofumi Yoshida*

*Dep. of Electronic Eng., Shizuoka University
3-5-1 Johoku Hamamatsu, 432, Japan
Tel : +81-53-478-1120 ; Fax : +81-53-475-0749

Abstracts This paper describes a DC voltage controller for the DC power supply which is constructed using the full-bridged MOS-FET DC-to-RF power inverter and rectifier. The full-bridged MOS-FET DC-to-RF inverter consisting of four MOS-FET arrays and an output power transformer has a control function which is able to control the RF output power when the widths of the pulse voltages which are fed to four MOS-FET arrays of the full-bridged inverter are changed using the pulse width control circuit. The power conversion efficiency of the full-bridged MOS-FET DC-to-RF power inverter was approximately 85 % when the duty cycles of the pulse voltages were changed from 30 % to 50 %. The RF output voltage from the full-bridged MOS-FET DC-to-RF inverter is fed to the rectifier circuit through the output transformer. The rectifier circuit consists of GaAs schottky diodes and filters, each of which is made of a coil and capacitors. The power conversion efficiency of the rectifier circuit was over 80 % when the duty cycles of the pulse voltages were changed from 30 % to 50 %. The output voltage of the rectifier circuit was changed from 34.7V to 37.6 V when the duty cycles of the pulse voltages were changed from 30 % to 50 %.

Keywords Inverter, MOS-FET, Pulse width control, Voltage control, Rectifier

1. INTRODUCTION

Among various types of high frequency MOS-FET inverters operating at short-wave frequencies, the full-bridged MOS-FET inverter is most important[1]-[4]. The full-bridged MOS-FET inverter generates an RF power when four MOS-FET arrays are switched. If a pulse width control circuit is used for the full-bridged inverter, the maximum RF output power is supplied from the full-bridged MOS-FET DO-to-RF power inverter when the inverter is driven by the normal drive signals, each having a duty cycle of 50 %. The RF output power fed from the full-bridged MOS-FET DO-to-RF power inverter decreases if the duty cycle decreases to less than 50 %[5]. The RF output voltage of the full-bridged MOS-FET DC-to-RF power inverter is rectified to obtain the DC voltage from the rectifier circuit, the output DC voltage level is controlled by changing the widths of the drive signals.

This paper describes the operation of the full-bridged MOS-FET DO-to-RF power inverter having both the pulse width control circuit and the rectifier circuit which rectifies the RF voltage to obtain the DC voltage.

2. CIRCUIT CONFIGURATION

Figure 1 shows the schematic diagram of the full-bridged MOS-FET DC-to-RF inverter with the pulse width control circuit.

Figures 2 shows the circuit diagrams of the pulse width control circuit, the drive circuit 1, the drive circuit 2, the main inverter circuit, and the rectifier circuit, respectively.

Figure 2 (a) shows the pulse width control circuit. The voltage controlled oscillator (VCO) of digital type is used to generate the drive signal at 1 MHz and the timing resistor is used to adjust the width of the pulse signal generated from the VCO. The output signal of the VCO is fed to the pulse width control circuit. The pulse width control circuit is composed of an integral circuit and a voltage comparator. The integral circuit simply consists of a resistor and a capacitor. The output signal is formed in triangular waveform in the integral circuit. the drive signals to be fed to the full-bridged inverter. When the pulse widths are changed, the turn-on times of the respective When the triangular waveform signal is fed to the voltage comparator, the voltage comparator controls the pulse widths of

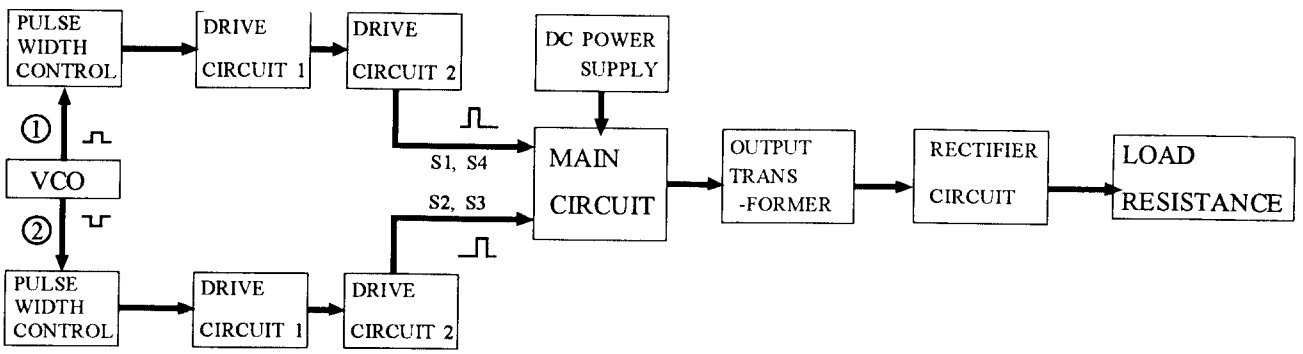
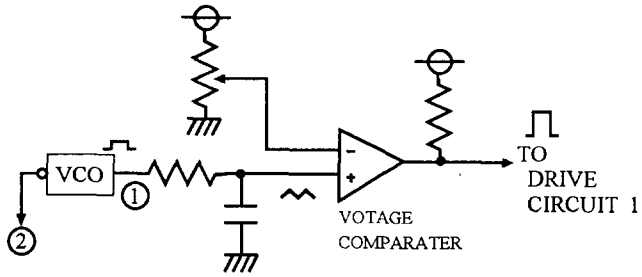
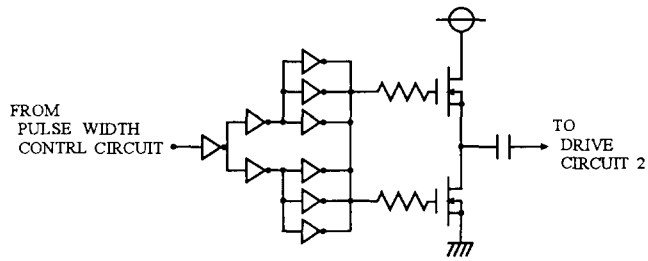


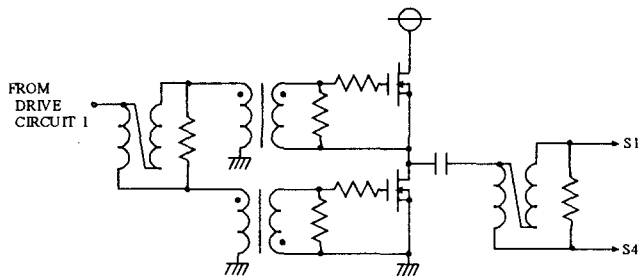
Fig. 1. Schematic diagram.



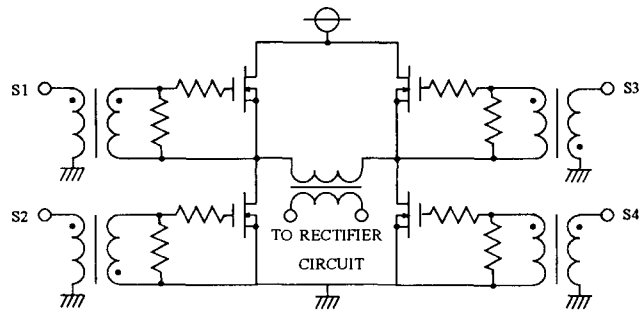
(a)



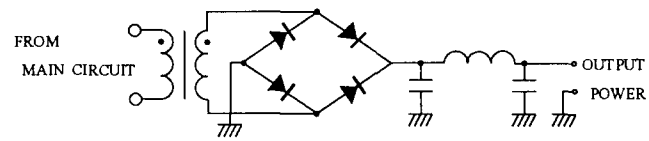
(b)



(c)



(d)



(e)

Fig. 2. Circuit diagram.
(a) Pulse width control circuit.
(b) Drive circuit 1.
(c) Drive circuit 2.
(d) Main inverter circuit.
(e) Rectifier circuit.

MOS-FETs in the full-bridged MOS-FET inverter are changed. These changes cause the RF output power to change.

Figure 2 (b) shows the drive circuit 1. The output signal of the pulse width control circuit shown in Figure 2 (a) is fed to the drive circuit 1. The drive circuit 1 is composed of buffers and a complementary power amplifier circuit. The output signal of the pulse width control circuit is fed to the complementary power amplifier circuit through the buffers. The complementary power amplifier circuit is composed of N-channel MOS-FETs (2SK416) and P-channel MOS-FETs (2SJ120). Tree MOS-FETs are connected in parallel to increase the handling power.

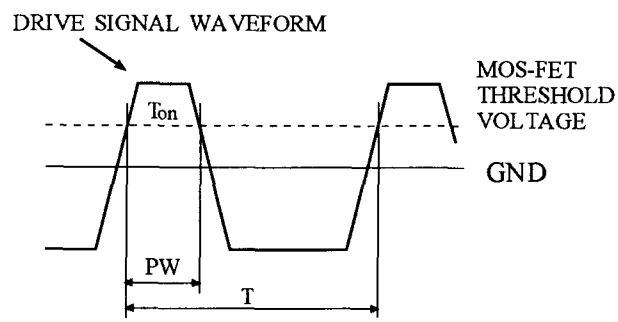
Figure 2 (c) shows the drive circuit 2. The output signal of the drive circuit 1 shown in Figure 2 (b) is fed to the drive circuit 2. The drive circuit 2 is composed of a power splitter consisting of a high frequency transformer and a half-bridged drive circuit. The output signal of the drive circuit 1 is fed to the half-bridge drive circuit through the power splitter. The half-bridged drive circuit is composed of two MOS-FETs (2SK409) connected in parallel to increase the handling power.

Figure 2 (d) shows the main inverter circuit. The output signal of the drive circuit 2 shown in Figure 2 (c) is fed to the main inverter circuit. The output signal of the drive circuit 2 is fed to four arrays of the full-bridge through the power splitter. Each array of the full-bridge is composed of four MOS-FETs (2SK1161).

Figure 2 (e) shows the rectifier circuit. The RF output power of the full-bridged MOS-FET DC-to-RF inverter shown in Figure 2 (d) is fed to the rectifier circuit through the output power transformer. The rectifier circuit is composed of GaAs schottky diodes and filters. The RF output power of the output transformer is fed to the load through the rectifier circuit consisting of GaAs schottky diodes and filters, each of which is composed of a inductor and a capacitor. The RF output voltage is rectified by the rectifier circuit and a DC voltage appears across the load.

3. DEFINITION OF DUTY CYCLE

Figure 3 illustrates the definition of the duty cycle of the drive signal waveform. When the full-bridged MOS-FET inverter is driven by the drive signal at high frequency, the turn-on and turn-off times of the RF output is affected by the drive signal waveforms at the gates of the respective MOS-FETs,



DUTY CYCLE (%) = PW / T X100

Fig. 3. Definition of the duty cycle of the driving signal waveform.

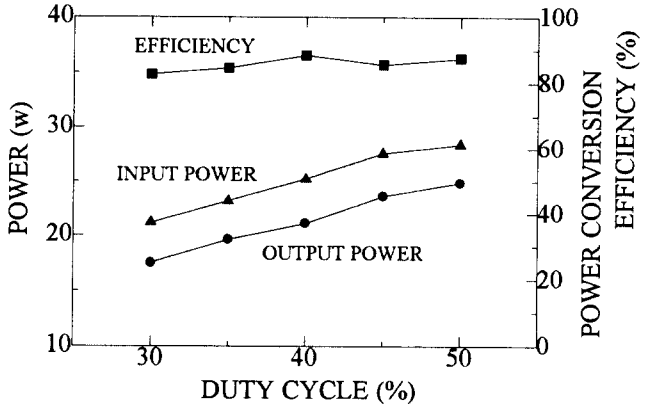


Fig. 4. RF output power and DC-to-RF power conversion efficiency of the full-bridged MOS-FET DC-to-RF inverter.

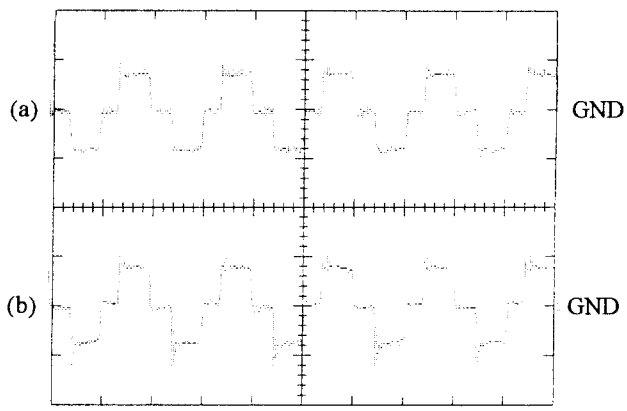


Fig. 5. Output voltage and current waveforms of the full-bridged MOS-FET DC-to-RF power inverter when the duty cycle is 30 %.
(a) Output voltage waveform. H : 500 ns/div., V : 50 V/div.
(b) Output current waveform. H : 500 ns/div., V : 1 A/div.

which are caused by the time delay at the edges of the gate drive voltages. In this paper, the ratio of the pulse width (PW) of the drive signal during which the MOS-FETs are kept turned on to the cycle time (T) of the drive signal is the defined as the duty cycle.

4. OPERATION

4.1. Full-bridged MOS-FET DC-to-RF power inverter

Figure 4 shows the RF output power and DC-to-RF power conversion efficiency of the full-bridged MOS-FET DC-to-RF inverter operating at a frequency of 1 MHz. In Figure 4, the RF output power was fed to a resistive load of 50 ohms through the output power transformer with a primary to secondary winding ratio of 1 to 1.

Figures 5 through 7 show the output voltage and current waveforms of the full-bridged MOS-FET DC-to-RF power inverter for a resistive load of 50 ohms. Figure 5 through 7 are respectively obtained when the duty cycle are 30 %, 40 %, and 50 %, respectively.

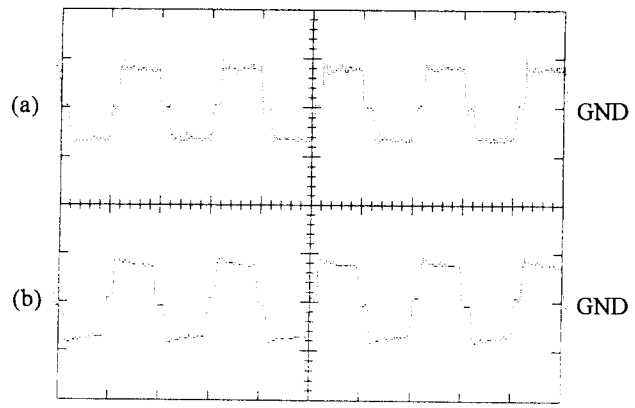


Fig. 6. Output voltage and current waveforms of the full-bridged MOS-FET DC-to-RF power inverter when the duty cycle is 40 %.
(a) Output voltage waveform. H : 500 ns/div., V : 50 V/div.
(b) Output current waveform. H : 500 ns/div., V : 1 A/div.

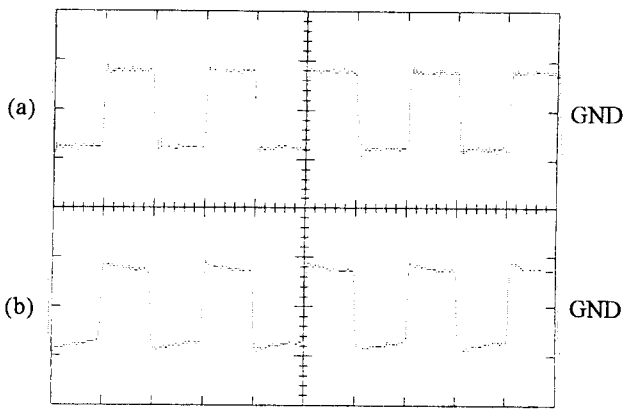


Fig. 7. Output voltage and current waveforms of the full-bridged MOS-FET DC-to-RF power inverter when the duty cycle is 50 %.
(a) Output voltage waveform. H : 500 ns/div., V : 50 V/div.
(b) Output current waveform. H : 500 ns/div., V : 1 A/div.

4.2. Output voltage of rectifier

Figure 8 shows the output voltage of the rectifier circuit when duty cycle is changed from 30 % to 50 %. In the measurement of the output voltage of the rectifier, two resistances of 50 Ω and 100 Ω were used as the load values. The output transformer used to feed the output of the full-bridged MOS-FET DC-to-RF power inverter to the rectifier circuit has a primary-to-secondary winding ratio of 1 to 1. The output voltage of the rectifier circuit was in Figure 8 controlled by changing the duty cycle.

Figure 9 shows the power conversion efficiency change when the duty cycle is changed. In the measurement of the performance of the rectifier circuit, resistances of 50 Ω and 100 Ω were used as the load values, and the output transformer used to feed the output of the full-bridged MOS-FET DC-to-RF power inverter to the rectifier circuit has a primary-to-secondary winding ratio of 1 to 1.

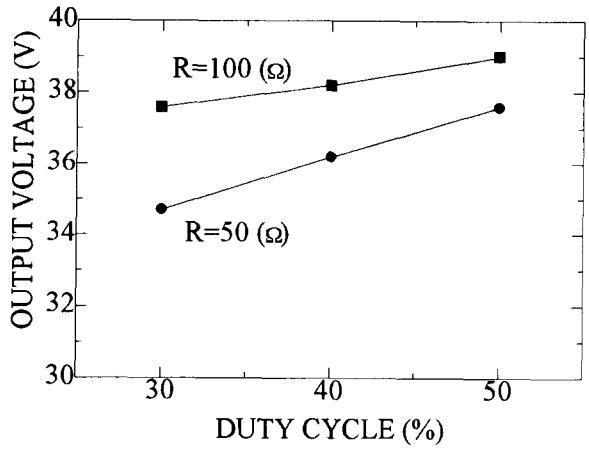


Fig. 8. Output voltage of the rectifier circuit when the duty cycle is changed from 30 % to 50 %.

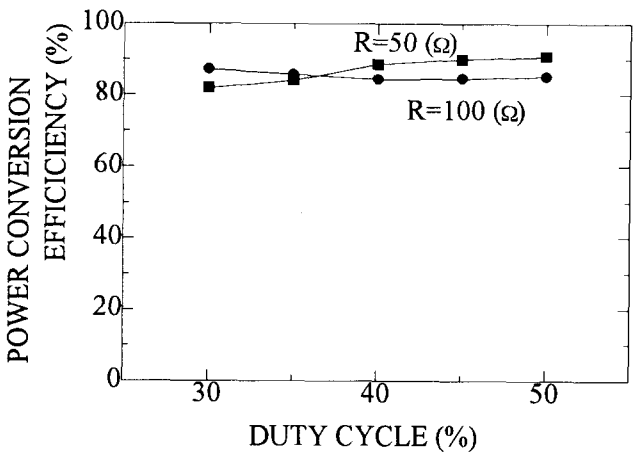


Fig. 9. Power conversion efficiency

5. CONCLUSION

DC voltages obtained from the voltage controller constructed using the full-bridged MOS-FET DC-to-RF power inverter and rectifier circuit were satisfactorily controlled by changing the duty cycle from 30 % to 50 %.

6, REFERENCES

[1] H.Ikeda, T.Suzuki, et al., "Online Output Measurement of Full-bridged MOS-FET RF power Inverter Operating at Shortwave Frequency", IEEE International Symposium on Industrial Electronics (ISIE '92), pp.711-744 (1992).

[2] H.Ikeda, T.Suzuki, et al., "Output power and Efficiency Tradeoff in full-bridged MOS-FET Power Inverter for Use at Shortwave Frequencies", IEEE IAS '91, pp.965-970 (1991).

[3] H.Ikeda, T.Suzuki, et al., "Power Conversion Efficiency in DC-to-RF MOS-FET High Power Inverter Operating at 2.5 MHz", IEEE ISCAS '91, pp.3035-3038 (1991).

[4] H.Ikeda, T.Suzuki, T.Nakabori, H.Yoshida, K.Honda, "Full-bridged MOS-FET DC-to-RF Power Inverter for Use with High-Frequency High-Power Ultrasonic Transducer", IEEE IECON '94, pp.108-111 (1994).

[5] Y.Ichioka, H.Ikeda, T.Suzuki, T.Nkabori, Y.Mizutani, H.Yoshida, "Full-Bridged MOS-FET DC-to-RF Inverter with Pulse Width Control Circuit", JIASC '95, pp.E-37 - E-40 (1995).