평균화 모델을 이용한 역률개선 제어기법

Power Factor Correction Technique of Boost Converter Based on Averaged Model

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Abstract

New power factor correction(PFC) technique based on the averaged model of boost converter is proposed. Without measurement of input current, power factor correction scheme derived from the averaged model is presented. With the measurements of input voltage and output voltage, the control signal is generated to make the shape of the line current same as the input voltage. The characteristincs of input line current distortion is analyzed by considering the generation of duty cycle.

I. Introduction

The boost converter is known as the most suitable configuration for power factor correction because its input current is continuous and can be shaped to track a desired waveform with minimum conducted noise[1]-[4]. Conventionally, with the measurement of input current, the boost converter input current is forced to track a given reference current waveform propotional to the input voltage by sensing the input current, comparing it with the reference current waveform. The circuit diagram of power factor correction boost converter and block diagram of PFC scheme for conventional PFC converter are presented in Figs. 1 and 2. The amplitude of the input current is controlled by the output voltage controller which regulate the desired output voltage. In this control structure, the measurement of input current is important factor. Therefore, the measurement method should be adequately fast to measure the variations in the line current as it tracks a sinewave within a power frequency cycle. To overcome this problem, a control method which can be used as power factor correction without instantaneous measurement of input line current was proposed in [5]. By the method used in [5], the high power factor can be obtained. However, in this control structure, the measurement of output load current should be made. This means another needs of current sensor although its response time may be slow. There are no guide line for controlling the output voltage of boost converter used in [5]. Therefore, in this paper, a simple new control method of power factor correcting boost converter without instantaneous measurement of input line current is proposed. With the measurements of only input voltage and output voltage, a high power factor and fast output voltage regulation can be achieved. By the computer simulations, the validities of proposed scheme are verified.

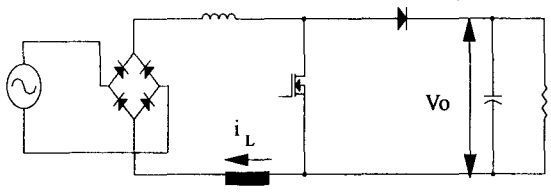

Figure 1: Circuit Diagram of Boost Converter

II. Power factor correction scheme

In deriving the expressions for the control strategy, the averaged model of boost converter is con-

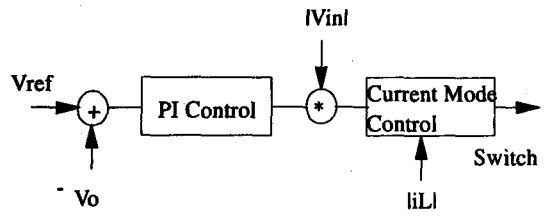

Figure 2: Diagram of Conventional PFC Scheme

sidered. To obtain the averaged model of boost converter, the switched model is considered at first. When the switch is on state, the state equation of boost converter can be expressed as follows:

$$\dot{X} = \begin{bmatrix} 0 & 0 \\ 0 & -1/(R_L C_o) \end{bmatrix} X + \begin{bmatrix} v_s(t)/L \\ 0 \end{bmatrix} \quad (1)$$

And, the state equation during the off status of switch can be obtained as follows:

$$\dot{X} = \begin{bmatrix} 0 & -1/L \\ 1/C_o & -1/(R_L C_o) \end{bmatrix} X + \begin{bmatrix} v_s(t)/L \\ 0 \end{bmatrix} \quad (2)$$

By appling averaging method to the above two equations during the switching period, the averaged model of boost converter can be obtained. The averaged model of boost converter with duty ratio as a control input can be derived as follows:

$$\dot{X} = \begin{bmatrix} 0 & -(1-d)/L \\ (1-d)/C_o & -1/(R_L C_o) \end{bmatrix} X + \begin{bmatrix} v_s(t)/L \\ 0 \end{bmatrix} \quad (3)$$

where, $X = [i_L(t)\ v_o(t)]^T$, and d is the duty ratio during the switching period. By assuming the desired inductor current waveform as

$$I_{desired}(t) = I sin(wt) \quad (4)$$

the required duty ratio can be derived as follows from equation (3):

$$d = 1 - \frac{v_s(t)}{v_o(t)} + \frac{LIw}{v_o(t)} cos(wt) \quad (5)$$

By making the inductor current waveform as equation (4), the high power factor can be obtained. The informations required for high power factor operation from equation (5) are only the input voltage and output voltage. Therefore, by the control law in equaiton (5), high power factor without instantaneous measurement of input line current can be obtained.

III. Cusp Distortion

It is noted that d is constrained to take values only between 0 and 1. By replacing the source voltage $v_s(t)$ by $V_p sin(wt)$ in equation (5), the following equation can be obtained.

$$d = 1 - \frac{V_p}{v_o(t)} sin(wt) + \frac{LIw}{v_o(t)} cos(wt) \quad (6)$$

The block diagram of proposed duty generator used for power factor correction is presented in Fig. 3. The constraint $d \leq 1$ implies

$$tan(wt) \geq \frac{LIw}{V_p}. \quad (7)$$

The equation (7) means the conditions for perfect tracking of the line current to be the desired current. To obtain the perfect tracking of input current, the desired current I and inductor value L should be small. However, it is impossible to satisfy the condition (7) at the start of the half power cycle. This means that there are some cusp distortion in input current waveform. From the constraint $d \leq 1$, the following condition of duty cycle can be obtained.

$$\begin{aligned} d = &\quad 1, && 0 \leq \theta \leq \theta_1 \\ = &\quad 1 - \tfrac{V_p}{v_o(t)} sin(\theta) + \tfrac{LIw}{v_o(t)} cos(\theta), && \theta_1 \leq \theta \leq \pi \end{aligned}$$

where $\theta_1 = tan^{-1}(\frac{LIw}{V_p})$. The effect of cusp distortion imposed by the proposed control law is illustrated in Table I for a typical parameter. Listed in this table are the resulting power factor and the third and fifth harmonic contents of the line current for a range of values of inductance L. As the value of inductance is increasing, the harmonic distortion of input current is also increasing.

TABLE I
Effect of Cusp Distortion

L(mH)	third harmonic (%)	fifth harmonic (%)	Power Factor
1	0.9	1.7	0.99
5	4.6	2.5	0.99
10	8.3	3.9	0.98

IV. Output voltage regulation

The output voltage regulation can be achieved by controlling the variable I which is the amplitude of desired line current command. It is required

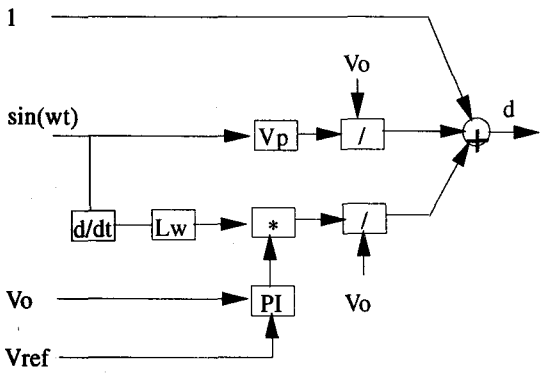

Figure 3: Duty cycle generator of the proposed control method

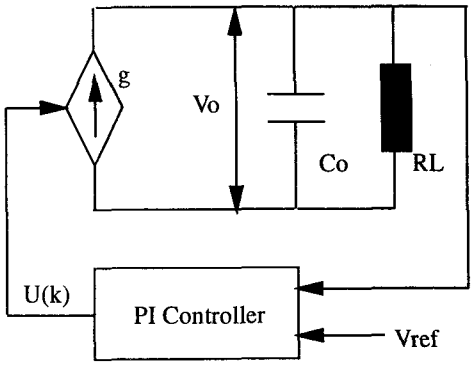

Figure 4: Block diagram of output voltage control loop

for high power factor operation and to guarantee the fast output voltage dynamics that the current command should be kept constant during the half period of source line waveform. Therefore, it is adequate to use the descrete time domain control method for output voltage regulation. Shown in FIg. 4 is the block diagram of output voltage control loop. To obtain the discrete time domain state model, the followings are assumed.

1) Output filter capacitance is adequately large so that the output voltage can be considered as constant over a half power cycle period.

2) The current flowing through output filter capacitor and load is dc component. This means that the high frequency component is rejected by the large output capacitance.

3) The current dymanics is so fast that the inductor current is same as the current command driven by output voltage controller.

With the assumptions 1), 2), and 3) above, the discrete time domain state equation during the positive half cycle can be described as:

$$V(k+1) = DV_o(k) + gR_L(1-D)U(k) \qquad (8)$$

where, D is e^{-T/R_LC_o}, g is $2V_P/(\pi V_o)$ which is a gain factor compensating the deference between current command and real current flowing to output filtor side, and $U(k)$ is the current command driven by output voltage controller at k-th time. The control input, $U(k)$ can be designed with suitable controller. In this paper, the analysis and design of output voltage controller are carried out using PI controller. By the PI controller, the control input $U(k)$ can be specified as follows:

$$U(k) = K_p e(k) + K_i \sum_i^k e(i) \qquad (9)$$

where $e(k)$ is the error between the voltage reference, V_{ref} and output voltage at k-th time. From (6) and (7), the transfer function of the closed-loop system is

$$T(z) = \frac{v(z)}{V_{ref}(z)} = \frac{G_c(z)G(z)}{1+G_c(z)G(z)} \qquad (10)$$

$$= \frac{gR(1-D)(K_p+K_i)z - gR(1-D)K_p}{z^2 + [gR(1-D)(K_p+K_i) - 1 - D]z + [D - gR(1-D)K_p]}. \qquad (11)$$

The characteristic equation becomes

$$CH(z) = z^2 + [gR(1-D)(K_p+K_i) - 1 - D]z + [D - gR(1-D)K_p]. \qquad (12)$$

V. Simulation Results

A simple PFC scheme controlled using the control law (5) was simulated and the results of the simulation are presented in Figs. 5 and 6. In performing the simulation, the effect of the load and output capacitor on the PFC voltage was considered by including a state equation. The basic model of the PFC boost converter used in the simulation is summarized by the following equation.

$$\frac{d}{dt}\begin{bmatrix} i_L \\ v_o \end{bmatrix} = H\begin{bmatrix} i_L \\ v_o \end{bmatrix} + \begin{bmatrix} 1/L \\ 0 \end{bmatrix} v_s \qquad (13)$$

where v_s and v_o are the instantaneous values of the input and the output voltage and H is the state

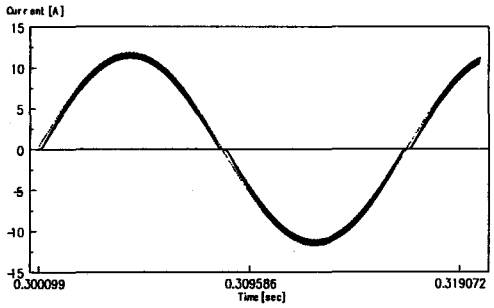

Figure 5: Waveforms of input current command and real input curent

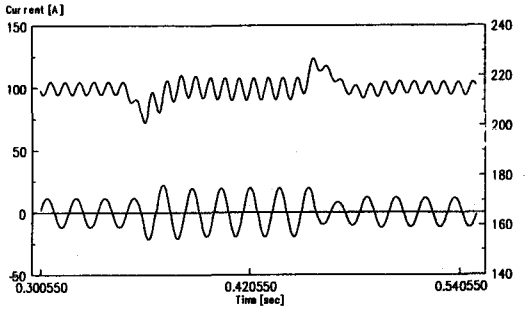

Figure 6: Waveforms of output voltage and input current with the step load change

feedback matrix:

$$H = \begin{bmatrix} -R_1/L & -1/L \\ 1/C & -1/R_L C_o \end{bmatrix} \quad (14)$$

when the switch is open and

$$H = \begin{bmatrix} -R_1/L & 0 \\ 0 & -1/R_L C_o \end{bmatrix} \quad (15)$$

when the switch is closed. where R_1 are the resitors in series with L modeling the power losses in the boost ocnverter.

Shown in Fig. 4 is the steady-state trace of the input line current for 1kW load. The actual line current is observed to track the desired input current waveform. Therefore, it is expected that high power factor can be obtained by the proposed method. Shown in Fig. 5 is the transient response of the output voltage and the input line current for step load changes between 500W to 1kW, and vice verse. The trace of output voltage response reveals the fast regulation for step load changes. This features can be designed with pole assignment technique.

VI. Conclusion

A new simple control scheme for the power factor correction boost converter which eliminates the need for instantaneous measurement of the line current is proposed in this paper. Using the averaged model of the boost converter, the control scheme is generatedto obtain high power factor while guarateeing fast output voltage regulation. Simulation results are presented to show the steady-state response and the transient response with step load changes. It is shown that the line current waveform can be shaped to track the input voltage waveform. Therefore, high power factor above 0.95 can be obtained. By varying the amplitude of desired current driven by output voltage controller, it is shown that fast output voltage regulation can be achived. It is expected that the proposed control scheme is useful for the digitally controlled high power factor converter.

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