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고역률과 고효율을 갖는 새로운 단일 전력단 AC/DC 컨버터

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A New Single Stage AC/DC Converter with High Power Factor and High Efficiency

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Abstract : A new single stage AC/DC converter with a high power factor is proposed. The proposed converter gives good power factor correction, low current harmonic distortions, and tight output regulations. This converter also has an high efficiency by employing Active-clamp method and synchronous rectifiers. To verify performances of the proposed converter, 90W-converter is designed. This prototype meets the IEC555-2 requirements satisfactorily with nearly unity power factor.

1. Introduction

Owing to the growing concern regarding harmonic pollution of the power distribution systems, and the adoption of standards such as IEC555-2, there is a need for single phase converters whose AC line current are low in harmonics and have power factor close to unity[1]. To meet the requirements, it is customary to add a power factor corrector ahead of the isolated DC/DC converter section of the switching power supply. The electrical performance can be acceptable, but the power factor corrector increases the size and cost of the power supply. In addition to those drawbacks, the overall efficiency decreases due to the losses of each stage. In order to keep the size and cost increase within acceptable limit, many efforts have attempted to integrate the functions of power factor correction and isolated DC/DC conversion into single stage[3-5]. Unfortunately many solutions suffer from large 120Hz voltage ripple at the output and low efficiency due to hard switching.

In this paper a new converter, which is capable of drawing a high quality current waveform from AC power supply operated in a discontinuous conduction mode and a pure DC output voltage without any harmonics voltage ripple. Moreover, based on Active clamp method and Synchronous rectifiers, the proposed converter achieves a high efficiency[6-8].

2. proposed converter

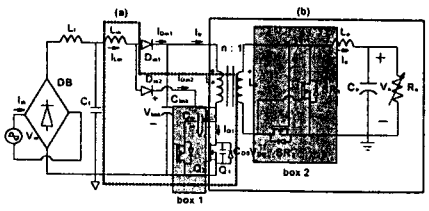

Fig. 1 Proposed converter (a)Boost stage, (b)Forward stage

Fig. 1 shows a single stage converter with a high power factor and a high efficiency. This converter can be understood as a cascade connection of a Boost converter in the dotted line followed by a forward converter in a solid line. The two converters share the same switch. The Active clamp method is shown in the shaded box 1. This Active clamp circuit provides the benefits of recycling the transformer leakage energy while minimizing turn_off voltage stress and means of achieving zero voltage switching(ZVS) for the switch Q_1. This results in decresing switching loss. The higher efficiency will be achieved by employing synchronous rectifiers in the shaded box 2. In this way the almost constant diode voltage (V_{DN}) is substituted by a resistance type (R_{DSON}). Therefore the overall efficiency of converter can be incresed.

3. Principle of operation

Fig. 2 illustrates the equivalent circuits and fig. 3 does the key waveforms for the proposed converter. Before describing the operation, the following assumptions are made.

- The input voltage, V_{in} is the constant DC voltage source.
- The clamp capacitor, C_{link} is so large for V_{link} to be a constant DC voltage.
- The switchs, Q_1 and Q_2 are ideal except for the output voltage capacitances and the body diodes.
- The leakage inductances and the parasitic capacitance are ignored in the power transformer.

T_0 - T_1 (M_1) : On state of Q_1

At T_0, the main switch Q_1 is on, the inductor L_{in} of Boost stage is linearly charge with the slope of $|V_{in}|/L_{in}$, and the voltage of inductor L_{in} is as can be seen in fig. 2-(a). This result in reversing the diode D_{in1} and the link capacitor C_{link}. transfers an energy to the output stage through transformer.

T_1 - T_2 (M_2) : (V_{DS} < $|V_{in}|$)

Q_1 is turned off at T_1. The output capacitance of Q_1, C_{1N} is charged by magnetizing current. The slope of the current of the boost stage inductor I_{Lin} is ($|V_{in}|$ - V_{1N}) / L_{in} decreases but the current still increases. Because the primary of the transformer is also still positive, C_{link} transfres an energy to the ouput stage.

T_2 - T_3 (M_3) : ($|V_{in}|$ < V_{DS} < V_{link})

The slope ($|V_{in}|$ - V_{1N}) / L_{in} decreses to negative and I_{Lin} starts to decrease. Other operations are the same as Mode 2.

T_3 - T_4 (M_4) : (V_{link} < V_{DS} < V_{Cc})

When V_{1N} is charged to V_{link}, the output stage is separated and the slope of V_{DS} decreses because only small magnetizing current remains to charge C_{1N}. The output inductor L_o freewheels through MOSFET SR_1 used for synchronous rectifiers and its slope is negative

T_4 - T_5 (M_5) : absorbing the transformer magnetizing energy

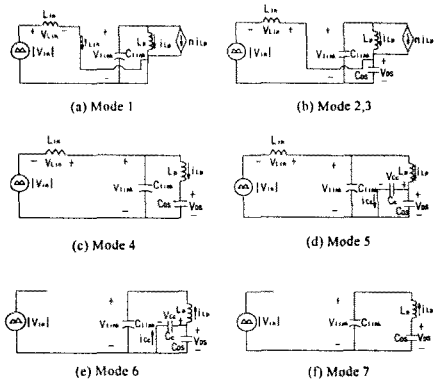

Fig. 2 Equivalent circuits of the proposed converter

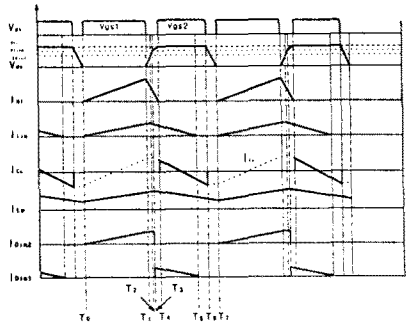

Fig. 3 Key waveforms

When V_{DS} is charged to V_{Cc}, the anti-parallel diode of Q_2 starts to conduct and V_{DS} is fixed to the voltage of clamp capacitor V_{Cc}. This results in reduction of the voltage stress of Q_1. The magnetizing current flows in a resonant manner by clamp capacitor C_c and the sum of magnetizing and leakage inductance, L_m+L_{dkg}. During this mode D_{in2} is reverse biased because $|V_{in}|+V_{link}$ is smaller than V_{Cc}.

T_5 - T_6 (M_6) : DCM of I_{Lin}

The current flowing in L_{in} decreases to zero and D_{in1} is reverse biased to separate the forward stage. The magnetizing current flows in a resonant manner from C_c to transformer through the auxiliary switch Q_2 which is turned on during Mode 5. In order to Q_2 to achieve ZVS, the device must be turned on before the clamp capacitor current, I_{Cc} is reverses direction.

T_6 - T_7 (M_7) : Dissipating the output capacitance energy of Q_1

To turn off the auxiliay switch Q_2 stops dissipation of C_C and changes the resonation from C_C and L_m+L_{dkg} to C_{DS} and L_m+L_{dkg}. C_{DS} is sufficiently small that it leades to an approximately linear discharging characteristic and the discharging time is very brief. When V_{DS} decreases to zero, the ZVS condition .of Q_1 is achieved.

4. analysis

4.1. Output voltage ripple

Fig. 4 shows the computer simulation about BIFRED and the proposed converter. It can be seen that BIFRED has considerably large 120Hz output voltage ripple but the converter does not. As can be seen the output voltage ripple of the proposed converter is much smaller than that of BIFRED.

4.2. Steady state analysis

The link capacitor voltage, V_{link}, the input RMS voltage V_{inrms} and the output voltage V_o have a relationship such as eq. 1 and 2.

$$V_o = \frac{DV_{link}}{n}$$

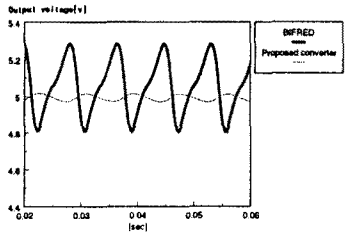

Fig. 4 Output voltage ripple of BIFRED and proposed converter

$$\frac{V_{link}}{V_{inrms}} = \frac{1}{\sqrt{2}}\left(1+\sqrt{1+\frac{0.852n^2V_o}{L_{in}f_sI_o}}\right) \quad (2)$$

From eq. 1 and 2 the steady state output voltage is obtained as a function of the input RMS voltage in eq. 3 As can be seen this funcution is a nonlinear equation to the input RMS voltage.

$$V_o = \left[\frac{0.426V_{inrms}^2D^2}{L_{in}f_sI_o} + \frac{\sqrt{2}V_{inrms}D}{n}\right] \quad (3)$$

5. Design

5.1. Inductor L_{in} and transformer turns ratio n

Refering to eq. 4, the proposed converter operates in DCM provided that I_{Lin} reaches to zero before the end of the switching period, T_s. This can be expressed as

$$T_{off} < (1-D)T_s \quad (4)$$

where T_{off} is off_time of Q_1.

Also eq. 5 provides the relationship of L_{in} and the peak current of this inductor I_{Linpk}.

$$I_{Linpk} = \frac{(V_{inpk}-V_{link})T_{off}}{L_{in}} \quad (5)$$

where V_{inpk} is the peak input voltage.

Thus, given input voltage, duty ratio and output conditions, n, V_{link} and L_{in} can be determined by solving eq. 1, 2 and 5 simutaneosly.

5.2. switch selection

The peak clamp capacitor voltage in the steady state, V_{Cc} can be obtained as followings.

$$V_{Ccpeak} = \frac{V_{link}}{1-D} \quad (6)$$

From this equation the peak voltage stress on the main switch Q_1, V_{DSpk} can be expressed as

$$V_{DSpk} = V_{Cc} \quad (7)$$

Main switch Q_1 is connected in parallel to improve the efficiency and endure the current stress. The choice of clamp Q_2 is less critical, as the clamp switch carries only small magnetizing current. Therefore the same kind of the main switch can be used as clamp switch.

5.3. Clamp capacitor, C_c and output inductor, L_o

The value of the clamp capacitor is determined by the clamp voltage ripple ΔV_{Cc} which will affect the peak voltage stress of the switches. The clamp capacitor is designed to meet the following condition.

$$V_{Cc} \gg \frac{T_{off}^2}{\pi^2(L_m+L_{dkg})} \quad (8)$$

And the output inductor can be selected as eq. 9.

$$L_o = \frac{(D-D^2)V_{link}T_s}{\Delta I_o} \quad (9)$$

6. Experimental results

To test the validaty of the proposed converter a 90W-converter was designed. Table 1 lists the components of the power stage for designs.

The exprimental waveforms of a input voltage, output voltage, input current, boost stage inductor current as well as link voltage are presented in fig. 5. Fig. 6 shows that ZVS is accomplished in the main switch Q_1.

Table 1 Components list of the prototype converter

Switching frequency(f_s)	100kHz
Min switch(Q_1)	2SK1816
Auxiliay switch(Q_2)	2SK1816
Boost stage inductor(L_m)	100μH
Clamp capacitor(C_c)	0.33μF
Link capacitor(C_{link})	220μF
Output inductor(L_o)	10μH
Output capacitor(C_o)	320μF
Diodes(D_{in1}, D_{in2})	S20L60
Bridge diode(DB)	D6SB60L
Filter inductor(L_f)	70μH
Filter capacitor(C_f)	0.1μF

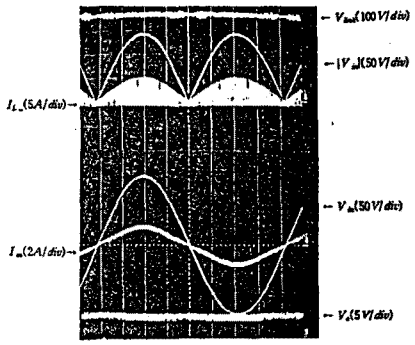

Fig. 5 Experimental waveforms of input/output voltage, input current, boost stage inductor current and link capacitor voltage

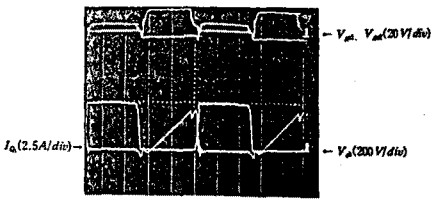

Fig. 6 ZVS of the main switch Q_1

6.1. Power factor and harmonic distortion

As the input curret waveform is not purely sinusoidal, it will contain harmonic distortion. The distortion is a fuction of the ratio of the peak line voltage(V_{lpk}) to the output voltage of the Boost stage(V_{link}) as follows[9].

$$PF = \frac{\sqrt{\frac{2}{\pi}} \int_0^{\pi} \sin\omega t \frac{G\sin\omega t}{1 - G\sin\omega t} d\omega t}{\sqrt{\int_0^{\pi} \frac{(G\sin\omega t)^2}{(1 - G\sin\omega t)^2} d\omega t}} \qquad (10)$$

where $G \equiv V_{link} / V_{inpk}$

Fig. 7 shows the calculated power factor using eq. 10 and the measured power factor under load variations. Fig. 8 shows the measured harmonics superimposed on specified IEC555-2 class D limits. These results show that the proposed converter meets the harmonic regulations and a measured power factor is above 0.965. The experimental waveforms of the input curmet and input voltage under load variations are shown in fig. 9.

6.2. Efficiency

Fig. 10 shows the efficeincy of the prototype converter as a function of output power. As can be seen, it has a high efficiency in a normal operation.

7. Conclusions

In this paper a new single-stage AC/DC converter for power factor correction is proposed. It gives a good power factor, low harmonic distortion and high efficiency as well as small output voltage ripple in a single stage. 90W-converter is designed and exprimented to test the validity of the proposed converter. This

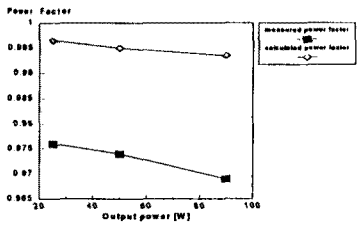

Fig. 7 Power factor under load variations

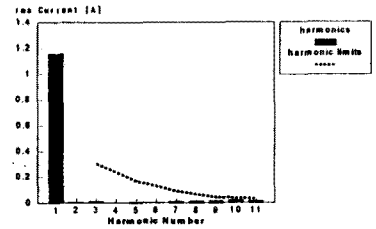

Fig. 8 The measured harmonics superimposed IEC 555-2 class D

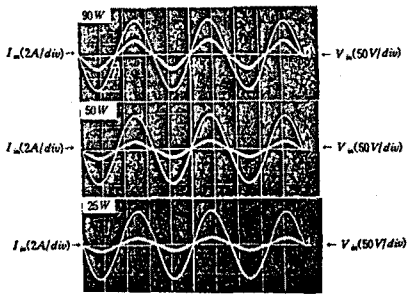

Fig. 9 Input currents and voltages under load variations

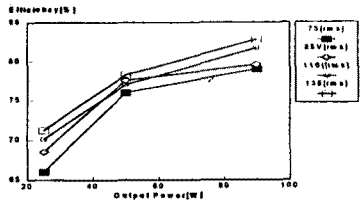

Fig. 10 Efficiency of the prototype converter under input voltage and output power variations

experimental results shows that the prototype of the proposed converter successfully meets the IEC555-2 requirements. The power factor is obtained above 0.965 and the efficiency around 80% in a normal operation. This converter is believed to be suitable for a low level power supply.

REFERENCES

[1] G. W. Moon, C. W. Rho, J. D. Bae, and M. J. Youn, High Power Factor Converter with Single-Switch Single-Stage. 1995, *Electronic Letters*, Vol 37, No 7, pp. 509-510

[2] P. Ericson, M. Madigan, and S. Singer, 1990, Design of a Simple High-Powe-Factor Rectifier Based on the Flyback Converter. *IEEE PESC*, pp. 792-801.

[3] E. X. Yang, Y. Jiang, G. Hua, and F. C. Lee, 1993, Isolated Boost Circuit for Power Factor Correction. *IEEE PESC*, pp. 196-203.

[4] M. H. Kheraluwala, A. Schnore, and R. L. Steigerwald, 1991, Performance Characterization of a High Power Factor Supply with a Single Power Stage. *IEEE PESC*, pp. 769-779.

[5] M. Madigan, R. Ericson, and E. Ismail, 1990, Integrated High Quality Rectifiers- Regulators. *IEEE PESC*, pp. 1034-1051.

[6] H. J. Ji, and H. J. Kim, 1994, Active Clamp Forward Converter with MOSFET Synchronous Rectification. *IEEE PESC*, pp. 895-901.

[7] R. Watson, F. C. Lee, and G. C. Hua, Utilization of an Active-Clamp Circuit to Achieve Soft Switching in Flyback Converters. 1994, *IEEE PESC*, pp. 909-916.

[8] J. A. Cobos, J. Sebastian, and J. Uceda, Study of the Applicability of Self-Driven Synchronous Rectification to Resonant Topologies. 1992, *IEEE PESC*, pp. 933-940.

[9] D. Tsang, F. C. Lee, and M. M. Jovanovic, Feasibility Study of Single Stage PFC/Regulator. 1993, *Delta Electronic Industrial Co. LTD : Fellowship Report*