이동도갭 상태들의 수소화된 비결정 실리콘 전계효과 트랜지스터의 성능에 대한 영향

Effects of Mobility-Gap States on the Performance of a-Si:H Field-Effect Transistors

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Abstract

An accurate and efficient single-integral semi-numerical model is developed and applied to analyse effects of localized electronic states in the mobility gap on the drain-current versus gate-voltage characteristics of hydrogenated amorphous field-effect transistors. It is shown that the low-density deep-gap states distributed in the midgap also sensitively and largely influence the device electronic performance as well as the large-density tail states distributed near the conduction band edge.

1. Introduction

Hydrogenated amorphous silicon (a-Si:H) semiconductor materials are characterized by the existence of a large number of localized electronic states in the mobility gap, i.e., between the edges of the conduction and valance bands. These localized electronic states are continuously distributed throughout the mobility gap, and composed mainly of two different kinds of electronic states for undoped intrinsic materials. Namely, near-band-edge tail states and deep-gap dangling bond states. The former states arise from the electronic potential fluctuations within an amorphous material due to the lack of long-range order in the atomic matrix system [1], and reside near the mobility edges, almost exponentially tailing off from each mobility edge. On the other hand, the latter states arise from dangling bonds, singly or doubly occupied, of silicon atoms uncompensated by hydrogen atoms, and produce an extensively broad distribution over a wide range of energy in the midgap with their density relatively low. For a high quality a-Si:H material produced by rf glow discharge in SiH_4 gas, a very low density of deep-gap states of the order of 10^{15} $/cm^3$-eV is obtained in the midgap.

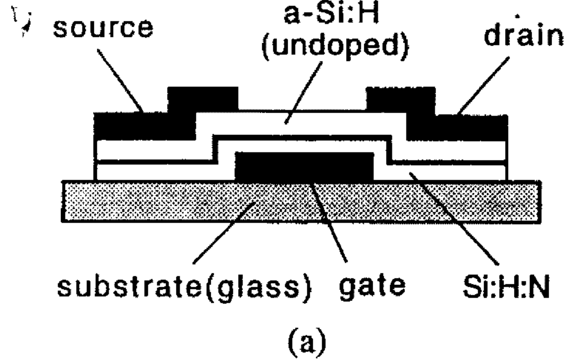
The large density localized states in the mobility gap greatly modify the electronic performance of a field-effect transistor (FET) by acting as an efficient source of trapping conduction electrons induced in the channel. Because of the higher electron mobility and the larger density distribution of donor-like localized states below the midgap, a-Si:H FETs are usually fabricated using undoped materials for the semiconductor and operated in the electron accumulation mode. The effective channel electron mobility of these devices is in the range 0.2-1.0 cm^2/V-s [2,3], which is relatively low compared with those FETs fabricated with CdSe, polycrystalline Si, or laser-annealed Si. However, a-Si:H FETs posses several superior advantages associated with the a-Si:H material, and are being utilized in the multiplex-addressing integrated circuits of LCD and image sensor devices.

The aim of this paper is twofold. The first is to present an accurate single-integral numerical model for the simulation of a-Si:H FETs (a double-integral formula is used usually [4]). The second is to apply this numerical model to analyse the effects of localized states in the mobility gap on the performance of a-Si:H FETs.

2. Device Modeling

The structure of an a-Si:H FET normally utilized in integrated circuits is schematically shown in Fig. 1, along with an energy band diagram for the device when a positive gate voltage has been applied with zero drain bias. In Fig. 1(b), the electric potential, $\phi(x)$, in the channel region near the semiconductor-insulator (Si:H:N) interface is measured from the conduction band edge (E_c) of the charge neutral semiconductor region electronically far away from the interface and thus

ϕ_s, the surface electric potential, will be positive in the normal electron accumulation mode of device operation. Also, E_v, E_f, V_{GS}, and V_i represent the energy at the valance band edge, the Fermi levels, the applied gate-source voltage, and the applied gate voltage drop across the insulator layer, respectively, and, additionally, q is the positive electronic charge.



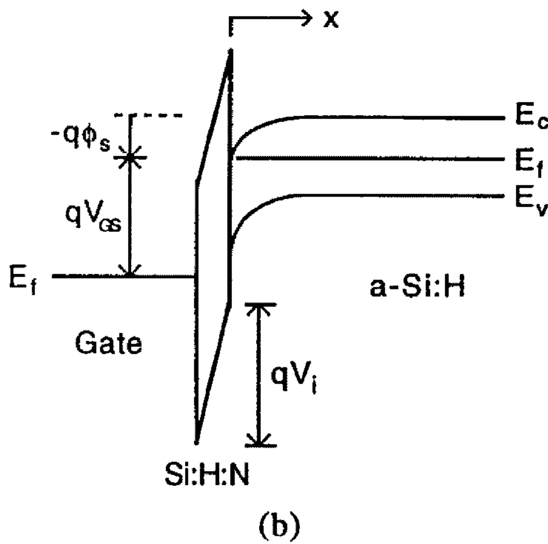


Fig. 1. (a) Cross-section of the structure of the a-Si:H FET, along with (b) the energy band diagram for a positive gate bias.

In an a-Si:H semiconductor-insulator system, the density distribution of localized states in the mobility gap near the interface is somewhat different from the distribution in the semiconductor bulk. FE and C-V measurements have revealed [5] that the density distribution of localized states in the upper half of the mobility gap can be described approximately with two exponential functions: one is for the deep-gap state distribution and another is for the tail state distribution. Mathematically, they can be expressed respectively by

$$G_d(E) = G_{dc}\, exp\left(\frac{E - E_c}{\alpha_d k_B T_o}\right) \tag{1}$$

and

$$G_t(E) = G_{tc}\, exp\left(\frac{E - E_c}{\alpha_t k_B T_o}\right), \tag{2}$$

where E refers to electron energy, k_B is the Boltzmann constant, T_o is the absolute lattice temperature, and G_{dc} and G_{tc} are the densities of $G_d(E)$ and $G_t(E)$ extrapolated to the edge of the conduction band, respectively. The quantities α_d and α_t are the coefficients of characteristic temperature for the exponential distributions of deep-gap states and tail states, respectively.

The localized electron concentrations occupied in the deep-gap states, n_d, and occupied in the tail states, n_t, at an arbitrary point inside the semiconductor are generally given by the definite integrals

$$n_d = \int_{E_v}^{E_c} G_d(E) f_{FD}(E)\, dE \tag{3}$$

and

$$n_t = \int_{E_v}^{E_c} G_t(E) f_{FD}(E)\, dE\,, \tag{4}$$

where $f_{FD}(E)$ is the distribution function of Fermi-Dirac statistics. Some new coefficients β_d and β_t are now introduced to define the effective temperatures of the localized electrons n_d and n_t in the channel region, where the electric potential is $\phi(x)$, by the following relations:

$$n_d = n_{do}\, exp\left[\frac{q\phi(x)}{\beta_d k_B T_o}\right] \tag{5}$$

and

$$n_t = n_{to}\, exp\left[\frac{q\phi(x)}{\beta_t k_B T_o}\right], \tag{6}$$

where the pre-exponential factors n_{do} and n_{to} are the localized electron concentrations in G_d and G_t under no bias condition, respectively. For a zero-temperature approximation for the electron occupation, $\beta_d=\alpha_d$ and $\beta_t=\alpha_t$ exactly. Otherwise, these coefficients may generally be a function of E_c-E_f and E_G=E_c-E_v in addition to α_d or α_t. However, for the high quality a-Si:H materials, grown by the PECVD, β_d is found to be approximately equal to α_d, and β_t to be very close to 1.1. The concentration of free electrons

occupied in extended states of the conduction band in the channel region is similarly given by

$$n_f = n_{fo}\, exp\left[\frac{q\phi(x)}{k_B T_o}\right], \tag{7}$$

where n_{fo} is the free electron concentration under no bias condition.

The electric field, F, in the channel region is obtained by the solution of Poisson's equation,

$$\frac{\partial F}{\partial x} = \frac{\rho(x)}{\varepsilon_s}. \tag{8}$$

Here $\rho(x)$ is the space-charge density and ε_s is the dielectric permittivity of a-Si:H. For a sufficient electric potential such that $q\phi(x) >> \beta_d k_B T_o$, the solution of Eq. (8) is analytically obtained with Eqs. (5)-(7) as

$$F = \sqrt{\frac{2k_B T_o}{\varepsilon_s}} \left\{ \begin{array}{l} \beta_d n_{do}\, exp\left[\dfrac{q\phi(x)}{\beta_d k_B T_o}\right] \\ + \beta_t n_{to}\, exp\left[\dfrac{q\phi(x)}{\beta_t k_B T_o}\right] \\ + n_{fo}\, exp\left[\dfrac{q\phi(x)}{k_B T_o}\right] \end{array} \right\}^{1/2}. \tag{9}$$

Therefore, the surface electric field induced at the interface is obtained by substituting the electric potential at $x=0$, i.e., ϕ_s into Eq. (9). Hence, the total electron charge induced into the semiconductor per unit area of interface above the gate is obtained easily by applying Gauss's law at $x=0$:

$$Q_s = -\sqrt{2\varepsilon_s k_B T_o} \left\{ \begin{array}{l} \beta_d n_{do}\, exp\left[\dfrac{q\phi_s}{\beta_d k_B T_o}\right] \\ + \beta_t n_{to}\, exp\left[\dfrac{q\phi_s}{\beta_t k_B T_o}\right] \\ + n_{fo}\, exp\left[\dfrac{q\phi_s}{k_B T_o}\right] \end{array} \right\}^{1/2}. \tag{10}$$

In order to balance charges, a sheet charge of the same magnitude, but a different sign, will, of course, be accumulated on the gate.

The total free electron charge induced in the channel region per unit area of interface above the gate is given by the integral

$$Q_f = -q\int_0^{\phi_s} n_f(\phi)\, F(\phi)^{-1}\, d\phi. \tag{11}$$

However, the evaluation of this integral by an analytic form is mathematically prohibited and, therefore, we possibly should resort on using a computer. Note that in Eq. (10), the 3rd term is apparently associated with the total induced free electron charge whereas the first two terms are apparently associated with the total induced localized charge. The free charge is relatively small compared with the total localized charge, unless the gate voltage is significantly large. Therefore, the free electron charge Q_f may be, but roughly, estimated from the total induced semiconductor charge Q_s, Eq. (10), by a Taylor series expansion of the square-root term. By introducing two empirical factors after the first-order Taylor series expansion, the total induced free electron charge has been analytically formulated in the following with good accuracy in a full range of Fermi level shifting almost to the edge of the conduction band for possible variations of material parameters:

$$Q_f = -\frac{\sqrt{2\varepsilon_s k_B T_o}\, n_{fo}}{\left\{ \begin{array}{l} \Xi_d(\phi_s)\, n_{do}\, exp\left[\dfrac{(1-2\beta_d) q\phi_s}{\beta_d k_B T_o}\right] \\ + \Xi_t\, n_{to}\, exp\left[\dfrac{(1-2\beta_t) q\phi_s}{\beta_t k_B T_o}\right] \end{array} \right\}^{1/2}}, \tag{12}$$

in which the two empirical factors are each defined by

$$\Xi_d(\phi_s) \equiv \frac{(2\beta_d - 1)^2}{\beta_d} \left\{ \begin{array}{c} 1 + \dfrac{2n_{fo}}{\beta_d n_{do}} \\ \times\, exp\left[\dfrac{(\beta_d - 1) q\phi_s}{\beta_d k_B T_o}\right] \end{array} \right\} \tag{13}$$

and

$$\Xi_t \equiv \frac{(2\beta_t - 1)^2}{\beta_t}. \tag{14}$$

Finally, under the assumption of a gradual channel, the applied gate voltage can be related to the applied drain voltage drop, $V(y)$, along the channel formed in the y direction between the source and the drain as follows:

$$V_{GS} \cong -\frac{Q_s}{C_i} + V_{FG} + V(y), \tag{15}$$

where C_i is the insulator capacitance per unit area and V_{FG} is the flat-band voltage. Then, the drain-to-source current of the a-Si:H FET is obtained by the single-integral equation

$$I_{DS} = -\frac{W\bar{\mu}_{eff}}{L}\int_{\phi_{sS}}^{\phi_{sD}} \Xi_V(\phi_s)Q_f(\phi_s)\, d\phi_s\,, \qquad (16)$$

where W is the gate width, L is the channel length, μ_{eff} is the effective band mobility of channel electrons averaged over the length of the channel, and ϕ_{sS} and ϕ_{sD} are the values of ϕ_s at the source, where $V(y)$=0, and at the drain, where $V(y)=V_{DS}$, the applied drain voltage, respectively. The factor $\Xi_V(\phi_s)$, dimensionless, is defined by

$$\Xi_V(\phi_s) \equiv \frac{dV(y)}{d\phi_s} = \frac{q\varepsilon_s}{Q_s} \times \left[n_{do}exp\left(\frac{q\phi_s}{\beta_d k_B T_o}\right) + n_{to}exp\left(\frac{q\phi_s}{\beta_t k_B T_o}\right) + n_{fo}exp\left(\frac{q\phi_s}{k_B T_o}\right) \right]. \qquad (17)$$

The drain current I_{DS} is taken to be completely saturated when the drain voltage V_{DS} exceeds the voltage difference V_{GS}-V_{FD}.

3. Numerical Analysis

The full drain-current versus gate-voltage characteristics of an a-Si:H FET can be provided with ease by evaluating the single-integral formula (16) numerically on a computer for various gate bias conditions using Eqs. (10), (12), (15), and (17). The numerical results for several different gate biases are shown for a device with the gate geometric ratio W/L=100 in Fig. 2. The material parameter values used are listed in Appendix, and it has been assumed for simplicity that V_{FB}=0 and $\mu_{eff}=\mu$, the bulk band mobility, throughout the present work. Also shown by a dashed curve in the same figure are the points of complete drain current saturation theoretically determined by the condition $V_{DS}=V_{GS}-V_{FB}$. It is first observed that a maximum drain current obtained by the device is on the order of 10 μA for the application of a considerably large gate voltage of 16 V. Since there exist exponentially distributed very large density tail states in the mobility gap near the conduction band edge, the Fermi level will be pinned by these tail states at large gate voltages and hence most of the applied gate field will be completely shielded, preventing the band from further bending at the semiconductor-insulator interface.

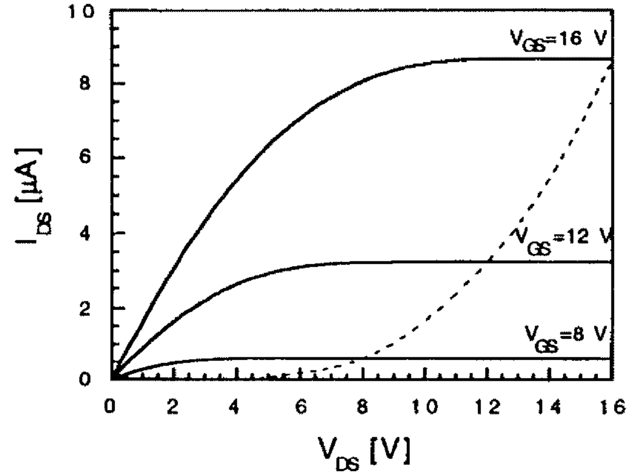


Fig. 2. Drain-current versus gate-voltage characteristics of the a-Si:H FET.

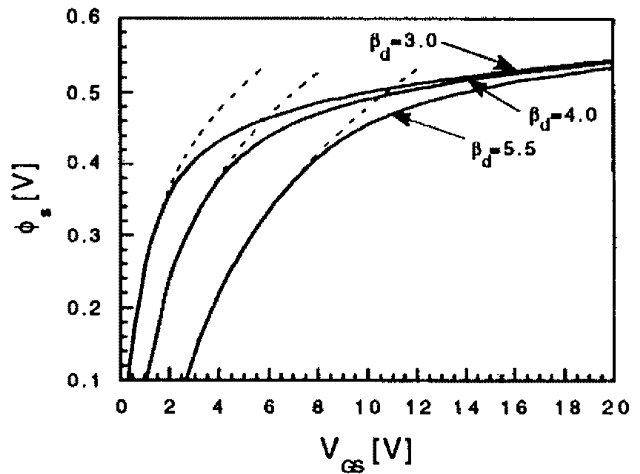


Fig. 3. Variations of the surface electric potential ϕ_s as a function of the applied gate voltage. β_t=1.1 for all the solid curves.

As shown by Fig. 3, the surface electric potential ϕ_s is almost constant even with significantly large gate voltages for all the three different cases in density distribution of deep-gap states, in contrast to the sharply increasing curves which all have been obtained under an assumption of no tail states in the mobility gap. Consequently, for an appreciable magnitude of drain current to be obtained, a large gate voltage must usually be applied in the a-Si:H FETs. For use as switching elements in the addressable LCD devices, the

minimum requirement for the drain current magnitude is considered to be about 5 μA. This magnitude of drain current is achieved in the figure at the drain and the gate voltages of approximately 10 V.

In the triode region the drain current of the device increases almost linearly with increasing drain voltage starting from zero. As the drain voltage is continued to increase further, the drain current becomes saturated smoothly and then is maintained constant. It is important to note that the drain current is already fully saturated much earlier than the theoretical saturation points determined by the condition $V_{DS}=V_{GS}-V_{FB}$. This may be a common feature of a-Si:H FETs since these devices are fabricated normally to operate in an accumulation mode and therefore a saturation of the drain current mainly occurs by the lack of enough free carriers available for electric conduction near the edge of the drain side channel.

Figure 4 shows the saturation drain current characteristics of a-Si:H FETs calculated as a function of the gate voltage for several different density distributions of deep-gap states. It is clearly noted that the saturation behavior of the drain current of an a-Si:H FET is also very sensitively affected by deep-gap states, although their density is low and they are distributed in the midgap. For the small changes in the value of β_d, the saturation drain current changes more than twice at a given gate voltage, and a smaller density of deep-gap states in the mobility gap results in a larger saturation drain current. This requests the use of a high quality material with low density deep-gap states for higher performance a-Si:H FET devices.

The effective field-effect mobility in an a-Si:H FET is a measure of the static and dynamic electronic performance of the device. This mobility is defined as the average single-carrier effective band mobility of all the induced carriers, including all the localized induced carriers in the mobility gap, all over the channel area. For an electrically efficient and speedy device, the effective field-effect mobility should be as high as possible. The calculated effective field-effect mobility for the a-Si:H FET simulated is shown in the two different device operation conditions as a function of V_{GS} in Fig. 5, where the mobility is normalized to the effective band mobility, μ_{eff}. In the low gate voltage region, the effective field-effect mobility increases very sharply, nearly exponentially, with the gate voltage, due to the low density distribution of the deep-gap states in the midgap. However, in the high gate voltage region, the mobility is saturated and almost constant, being independent of the gate bias, because of the Fermi level pinning by the high density tail states near the conduction band edge. The maximum values of mobility achieved are 0.8 cm^2/V-s for V_{DS}=50 mV and 0.5 cm^2/V-s on saturation, at the large gate voltage of 20 V. The saturation mobility is always smaller than that of the other case since the fraction of free electrons to total induced electrons in the channel will be always smaller near the drain side channel compared with the latter case. . The mobility difference in ratio at a given gate bias is noted to be significant in the low gate voltage region. This effect is, additionally, associated with the lower density distribution of the deep-gap states in the mobility gap in a high quality a-Si:H.

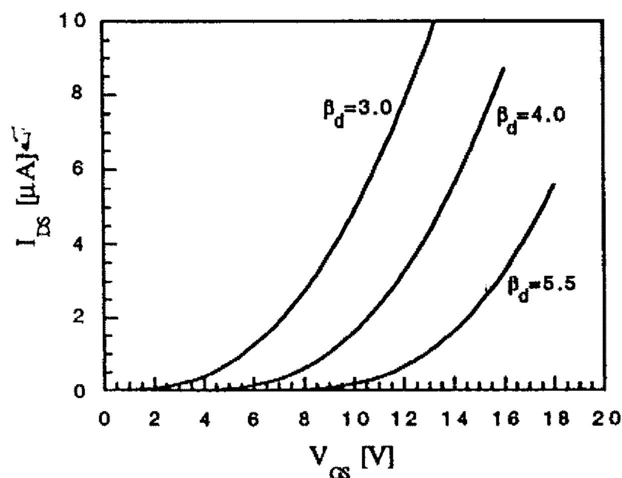


Fig. 4. Saturation drain current characteristics of a-Si:H FETs for several different distributions of deep-gap states in the mobility gap. β_t=1.1 for all three curves.

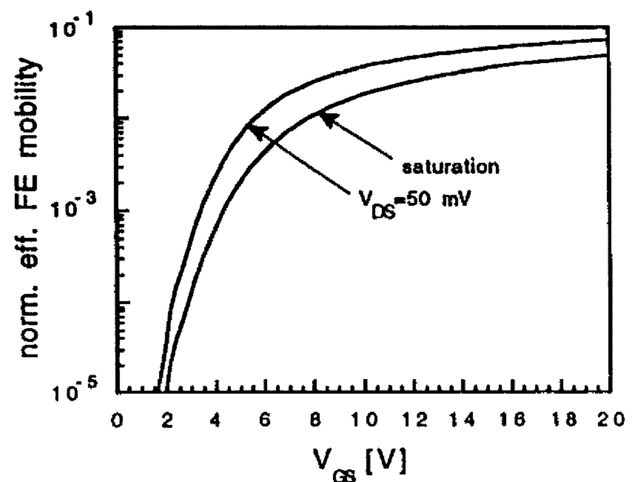


Fig. 5. Magnitudes of the effective field-effect mobility of the a-Si:H FET on drain current saturation and at a very small drain voltage.

4. Conclusion

The a-Si:H semiconductor have a large concentration of localized electronic states, composed mainly of deep-gap dangling-bond states and near-band-edge tail states, in the mobility gap. Their effects on the static electronic performance of a-Si:H FETs have been investigated using an accurate and efficient semi-numerical model developed in this work. It has been shown that most of the induced electrons in the channel are efficiently trapped by the localized states so that the electronic performance of the a-Si:H FETs is degraded greatly, and is influenced largely and sensitively even by different low-density distributions of dangling bond states in the midgap. It is suggested that high quality a-Si:H materials with low densities of deep-gap states and tail states be used in order to have higher performance a-Si:H FETs.

Appendix

T_o = 300 K
$E_f = E_c$-0.6 eV (bulk)
β_d = 4.0 (unless specified specifically)
β_t = 1.1
$C_i = 1.77\times10^{-4}$ F/cm^2 ($\varepsilon_s = 12\varepsilon_o$ for Si:H:N)
$\varepsilon_s = 12\varepsilon_o$
μ_{eff} = 10 cm^2/V-s
$n_{fo} = 1.0\times10^9$ /cm^3
$G_{dc} = 1.0\times10^{19}$ /cm^3-eV
$G_{tc} = 7.0\times10^{19}$ /cm^3-eV

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