[IV~15]

Effect of Si, Ge Pre-implant induced Defects on Electrical properties of P+-n Junctions during Rapid Thermal Annealing

K.I. Kim*, Y.K. Kwon*, W.J. Cho**, H. Kuwano***

* *Electronic device & system research Lab.*
Research Institute of Industrial Science & Technology
P.O. Box 135, Pohang, 790-600, Korea

** *Advanced process Tech. Dept. LG Semicon, Korea*
*** *Department of Electrical Engineering, Faculty of Science and Technology,*
Keio University, Japan

ABSTRACT

Recent developments in the downscalling of microelectronic devices have resulted in the adoption of Si, Ge ion implantation prior to shallow dopant implantation. the amorphous layer induced by these heavy and electrically neutral ions has been shown to eliminate dopant channeling in the tail region during shallow junction formation. However, ion implantation has serious disadvantage of creating a large amount of defects. All the defects introduced during the ion implantation and the subsequent processing considerably influence the electrical properties of device characteristics. Therefore, it is worthwhile to elucidate the structure and the nature of defects introduced by Si, Ge preamorphization and their effects on electrical characteristics. In this study, the annealing behaviors of Si, Ge pre-implant induced defects and their effects on the electrical properties of p+-n shallow junctions during RTA are investigated.