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Batching and Input Regulation in the Photolithography Process for Memory Chips Fabrication

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ABSTRACT

We consider the photolithography process for memory chips fabrication. Each wafer is processed at the same machine each time it reenters the process. A stepper in the process requires deliberate setup for processing each circuit layer. We investigate the batch sizes for the steppers. To do this, we use a simplified simulation model that aggregates the other fabrication processes into a single queueing station using the response time approximation technique. We also investigate input regulation policies for the photolithography process. Relationships between performance measures, batch sizes, and input policies are discussed using simulation experiments.