IMPLEMENTATION OF REAL TIME RELP VOCODER ON THE TMS320C25 DSP CHIP

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ABSTRACT

Real-time RELP vocoder is implemented on the TMS320C25 DSP chip. The implemented system is IBM-PC add-on board and composed of analog in/out unit, DSP unit, memoy unit, IBM-PC interface unit and its supporting assembly software. Speech analyzer and synthesizer is implimented by DSP assembly software. Speech parameters such as LPC coefficients, base-band residuals, and signal gains is extracted by autocorrelation method and inverse filter and synthesized by spectral folding method and direct form synthesis filter in this board. And then, real-time RELP vocoder with 9.6Kbps is simulated by down-loading method in the DSP program RAM.

I. INTRODUCTION

The residual excited linear prodictive (RELP) vocoder was originally proposed by Un and Magill [1]. The coder operates by generating the prediction error signal (or residual) obtained by inverse filtering the speech data using the LPC (Linear Prediction Coding) coefficients. A downsampled baseband residual is transmitted to the receiver together with the LPC coefficients where a full-band signal can be recovered by method of spectral folding and used as the excitation for an all-pole filter[1,3,8].The RELP algorithm produces good quality, natural sounding speech at 9.6Kbps[1,3]. This paper describes the design of a new compact,low cost RELP vocoder, implemented on a signgle board using TMS320C25 digital signal processor. The data rate of the vocoder is 9600bps with a frame size of 20ms(160 samples at 8KHz). The vocoder implementation divides into several subsystems: analog in/out, DSP, program memory,IBM-PC interface, and DSP assembly softwares.

II. RELP ALGORITHM

Analyzer

The block of analyzer is shown in Fig. 1. The input speech signal is digitized at a sampleing frequency of 8kHz and is preemphasized at approximately 6dB/octave (breaking point frequency=400Hz)[5]. Linear Prodiction (LP) analysis using the autocorrelation method is carried out on a frame-by-frame basis to extract ten LP coefficients for transmission. The analysis windows used is a overlapping hamming windows of 200 samples. Residuals is finded from inverse filter with LPC coefficients[1,2,5,8]. The extracted residual signal is low-pass filterd with a cutoff frequency of 800Hz and down-sampled 4 to 1 so that a baseband residual signal sampled at 1.6KHz results[5,6]. LPC coefficients, base-band residuals and gains are saved to memory for transmission.

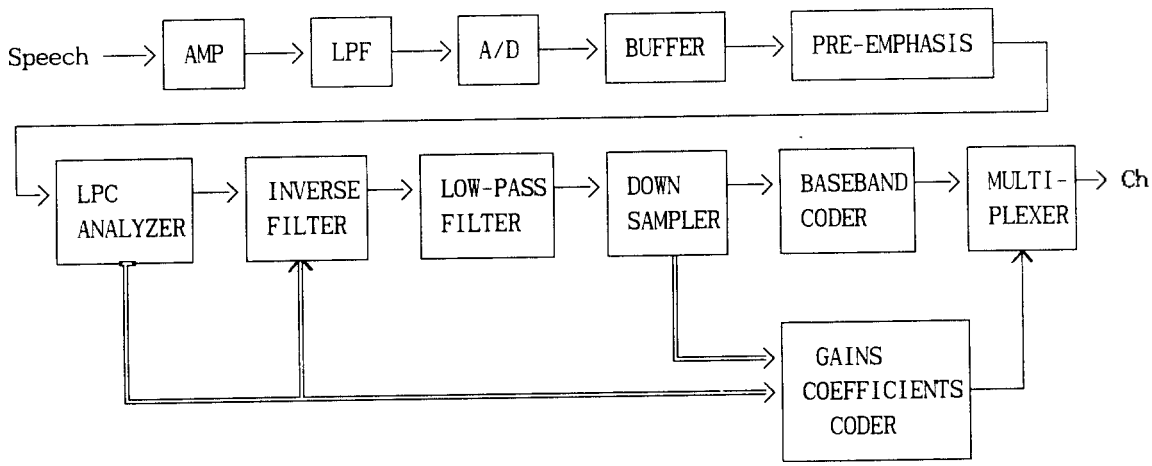


Fig. 1. RELP analyzer

Synthesizer

The block of synthesizer is shown in Fig. 2. The gains, coefficients and base-band residuals from channel is decoded and up sampled by zero insertion inter-polation[9] to produce full band excitation signal.

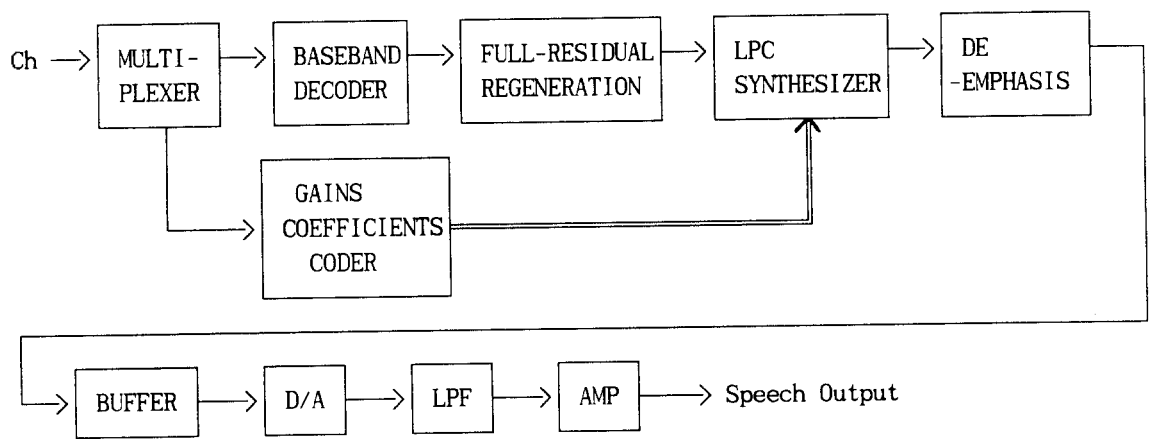


Fig. 2. RELP synthsizer

Direct form synthesis filter[7,8] is used for speech synthesis with LPC coefficients, full band excitation signals and gains. And deemphasizes at approximately 6dB/octave (breaking point frequency=400Hz) is processed.

$$S(n) = a(k)S(n-k) + e(n)$$

where, S(n) = nth sample value
a(k) = kth LPC coefficeint
e(n) = nth excitation signal

III. HARDWARE

The block diagram of hardware system is shown in Fig. 3. Hardware system is divided into several subsystems:analog in/out, DSP, program memory, and IBM-PC interface.

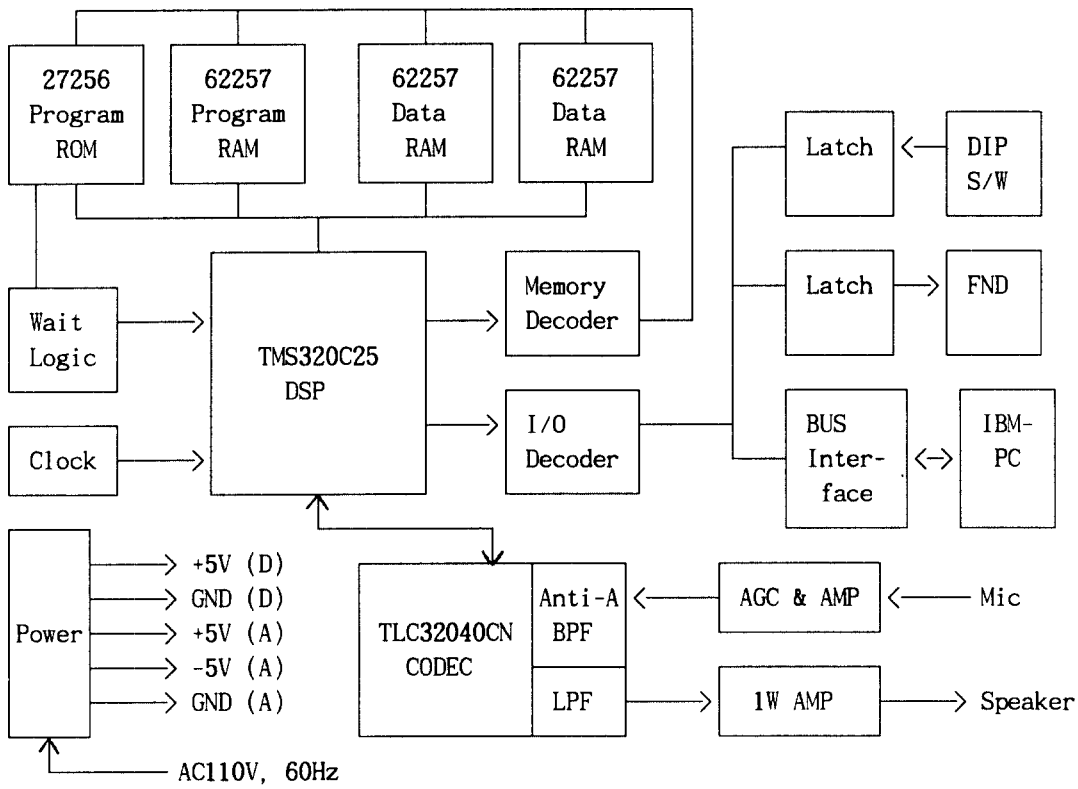


Fig. 3. Block diagram of hardware system

Analog In/Out

Input device of audio is 600 ohm microphone and output device 8 ohm speaker. Speech input signal is amplified to 6Vpp, and band-pass filtered by a anti-aliasing switched-capacitor filter, before being sampled and convered into a 14bit resolution 2's complement value. Output driver for speaker is used 1W operational amplifier. The used codec is TI's TLC32040CN and operate synchronously to TMS320C25 DSP chip, and sampling rates can be changed via DSP

control[13,14].

TMS320C25 DSP

The TMS320C25 Digital Signal Processor offers a cost-effective alternative to custom VLSI. It has the following significant key features[12].

- 100ns instruction cycle time
- 544 words of on-chip data RAM
- 4K words of on-chip ROM
- 128K words of data/program space
- single cycle multiply instruction
- 16-bit instuction and data words
- 32-bit ALU and accumulator
- 16-bit parallel shifter
- block moves for data/program
- serial port for direct codec interface
- three maskable interrupts
- On-chip clock generator
- CMOS,single 5-volt supply
- 68pin,40Mhz clock speed

Memory

Because TMS320C25 is running at 40MHz, quarter phase time Q is 25nsec, therfore, access time of DSP chip is 40nsec at no wait status. Memory decoder is implemented with PAL and wait circuit is composed of logics. Program memory is divided two part, one is two EPROM TMS27C256(120ns,8bitx32K) that is used for monitor program and has one wait cycle, another is two SRAM KM64257(35ns,4bitx64K) that is used for down-load program and has no wait cycle. Data memory also is implemented two SRAM KM64257 for 64K space.

IBM-PC Interface

The interface between IBM-PC and DSP board is composed of handshaking logics. IBM-PC requests to TMS320C25 by interrupt and TMS320C25 responds with XF and BIO signal to IBM-PC and then IBM-PC can have down-load function for real-time simulation. The structure of handshaking protocol frame is shown in Fig. 4.

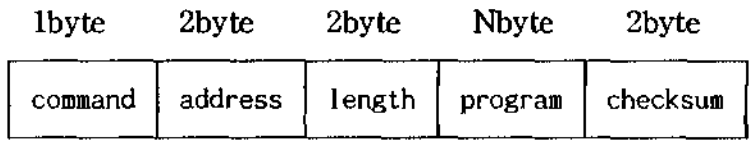


Fig. 4. Handshaking Frame Structure

IV. SOFTWARE

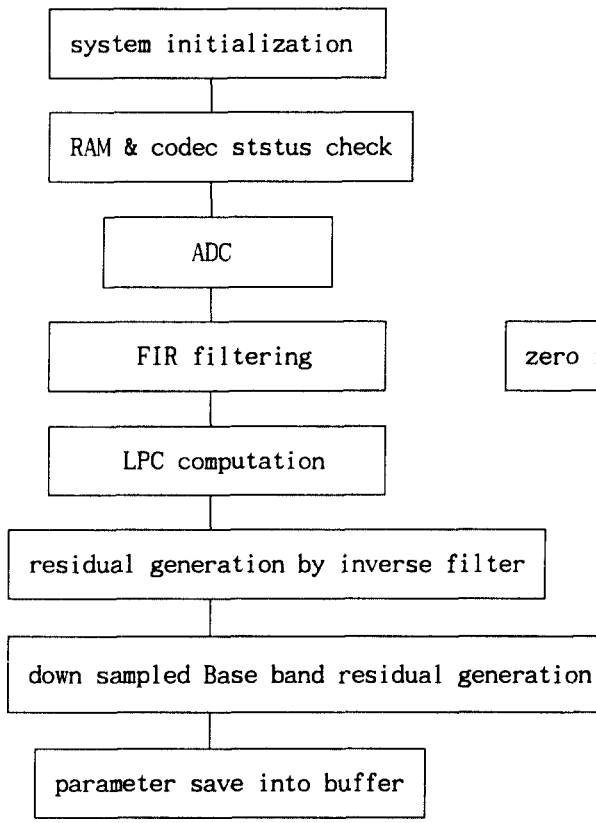
Monitor and Debugger

The program ROM of TMS320C25 Board has monitor and debugger. When assembly programs developed from IBM-PC is loaded down to TMS320C25's program RAM, it can be not only excuted on real-time, but also tested for

algorithm processing. The debugger has 16 functions to be controlled by IBM-PC command.

ROM Routine

The ROM hold a variety of speech processing routine such as A/DC, D/AC, FIR filtering, hamming windowing, autocorrelation, residual computation, base-band computation, ADPCM coder, direct form synthesizer, ADPCM decoder, real-time RELP vocoder processing, host interrupt test and initial system reset. The required function can be coded as a sequence of calls to those routines. The simulation routine for real-time RELP processing is shown in Fig. 5 and Fig. 6.



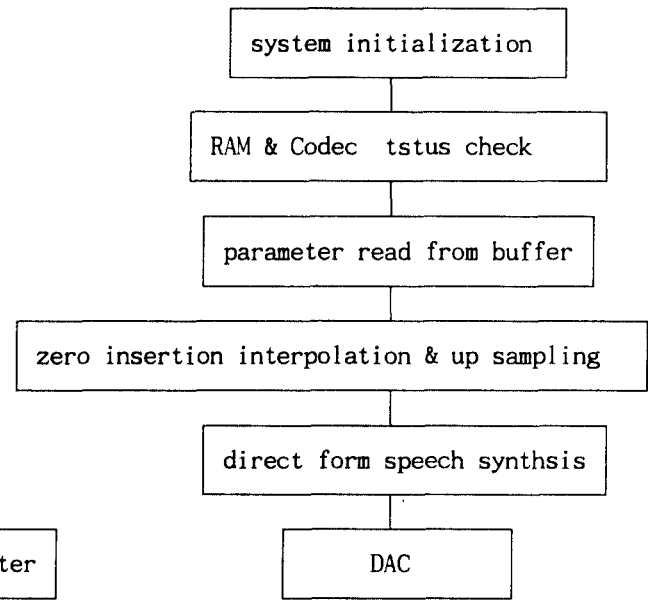


Fig. 6. Flowchart of the assembly program for RELP synthesizer

Fig. 5. Flowchart of the assembly program for RELP Analyzer

V. CONCLUSION

The RELP codec board is realized using about 31 ICs including the one DSP chip and mounted in a printed circuit board. Its dimension are 10x34 centi-meters. Real-time RELP vocoder is implemented on the TMS320C25 DSP chip. The implemented system is IBM-PC add-on board and composed of analog in/out unit, DSP unit, memoy unit, IBM-PC interface unit and its supporting assembly

software. And then, real-time RELP vocoder with 9.6Kbps is designed and implemented. This system can be easily modified for various application areas involving adaptive digital filter, adaptive noise canceller by down-loding into program RAM.

ACKNOWLEDGEMENT

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