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Hardware Approach to Fuzzy Inference — ASIC and RISC —

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Abstract†

This talk presents the overview of the author's research and development activities on fuzzy inference hardware. We involved it with two distinct approaches. The first approach is to use application specific integrated circuits (ASIC) technology. The fuzzy inference method is directly implemented in silicon. The second approach, which is in its preliminary stage, is to use more conventional microprocessor architecture. Here, we use a quantitative technique used by designer of reduced instruction set computer (RISC) to modify an architecture of a microprocessor.

In the ASIC approach, we implemented the most widely used fuzzy inference mechanism directly on silicon. The mechanism is beaded on a *max-min* compositional rule of inference, and Mandami's method of fuzzy implication. The two VLSI fuzzy inference chips are designed, fabricated, and fully tested. Both used a full-custom CMOS technology. The first chip was designed at the AT&T Bell Laboratories. The second and more elaborate chip was designed at the University of North Carolina(UNC) in cooperation with MCNC. Both VLSI chips had multiple datapaths for rule evaluation, and they executed multiple fuzzy if-then rules in parallel.

The AT&T chip is the first digital fuzzy inference chip in the world. It ran with a 20 MHz clock cycle and achieved an approximately 80,000 Fuzzy Logical Inferences Per Second (FLIPS). It stored and executed 16 fuzzy if-then rules. Since it was designed as a proof of concept prototype chip, it had minimal amount of peripheral logic for system integration.

UNC/MCNC chip consists of 688,131 transistors of which 476,160 are used for RAM memory. It ran with a 10 MHz clock cycle. The chip has a 3-staged pipeline and initiates a computation of new inference every 64 cycle. This chip achieved an approximately 160,000 FLIPS. The new architecture have the following important improvements from the AT&T chip:

- Programmable rule set memory (RAM).
- On-chip *fuzzification* operation by a table lookup method.
- On-chip *defuzzification* operation by a centroid method.
- Reconfigurable architecture for processing two rule formats.
- RAM/datapath redundancy for higher yield

It can store and execute 51 if-then rule of the following format:

IF A and B and C and D Then Do E, and
Then Do F.

With this format, the chip takes four inputs and produces two outputs. By software reconfiguration, it can store and execute 102 if-then rules of the following simpler format using the same datapath:

IF A and B Then Do E.

With this format the chip takes two inputs and produces one outputs.

We have built two VME-bus board systems based on this chip for Oak Ridge National Laboratory (ORNL). The board is now installed in a robot at ORNL. Researchers uses this board for experiment in autonomous robot navigation. The Fuzzy Logic system board places the Fuzzy chip into a VMEbus environment. High level C language functions hide the operational details of the board from the applications programmer. The programmer treats rule memories and fuzzification function memories as local structures passed as parameters to the C functions.

ASIC fuzzy inference hardware is extremely fast, but they are limited in generality. Many aspects of the design are limited or fixed. We have proposed to designing a fuzzy information processor as an application specific processor using a quantitative approach . The quantitative approach was developed by RISC designers

In effect, we are interested in evaluating the effectiveness of a specialized RISC processor for fuzzy information processing. As the first step, we measured the possible speed-up of a fuzzy inference program based on if-then rules by an introduction of specialized instructions, *i.e.*, `min` and `max` instructions. The *minimum* and

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maximum operations are heavily used in fuzzy logic applications as fuzzy intersection and union. We performed measurements using a MIPS R3000 as a base microprocessor. The initial result is encouraging. We can achieve as high as a 2.5 increase in inference speed if the R3000 had `min` and `max` instructions. Also, they are useful for speeding up other fuzzy operations such as *bounded product* and *bounded sum*.

The embedded processor's main task is to control some device or process. It usually runs a single or a limited number of programs. Tuning a general purpose embedded processor to create an embedded processor for fuzzy control is very effective.

Table I shows the measured speed of the inference by a MIPS R3000 microprocessor, a fictitious MIPS R3000 microprocessor with `min` and `max` instructions, and a UNC/MCNC ASIC fuzzy inference chip. The software that used on microprocessors is a simulator of the ASIC chip. The first row is the computation time in seconds of 6000 inferences using 51 rules where each fuzzy set is represented by an array of 64 elements. The second row is the time required to perform a single inference. The last row is the fuzzy logical inferences per second (FLIPS) measured for each device.

There is a large gap in run time between the ASIC and software approaches even if we resort to a specialized fuzzy microprocessor. As for design time and cost, these two approaches represent two extremes. An ASIC approach is extremely expensive. It is, therefore, an important research topic to design a specialized computing architecture for fuzzy applications that falls between these two extremes both in run time and design time/cost.

TABLE I
INFERENCE TIME BY 51 RULES

Time	MIPS R3000		ASIC
	Regular	With min/max	
6000 inference	125s	49s	0.0038s
1 inference	20.8ms	8.2ms	6.4μs
FLIPS	48	122	156,250

Reference

[1] Pin, F. G., H. Watanabe, J. R. Symon, and R. S. Pattay, "Autonomous Navigation of a Mobile Robot Using Custom–Designed Qualitative Reasoning VLSI Chips and Boards," Proc. of IEEE International Conference on Robotics and Automation, pp. 123–128, May 1992.

[2] Pin, F. G., H. Watanabe, J. R. Symon, and R. S. Pattay, "Using Custom–Designed VLSI Fuzzy Inference Chips for the Autonomous Navigation of a Mobile Robot," *Proc. of IEEE/RSJ International Conference on Intelligent Robots and Systems*, pp. 790–795, July 1992.

[3] Togai, M. and H. Watanabe, "A VLSI Implementation of Fuzzy Inference Engine: Toward an Expert System on a Chip," *Information Sciences: An International Journal*, Vol. 38, PP. 147-163, 1986.

[4] Togai, M. and H. Watanabe, "An Inference Engine for Real-time Approximate Reasoning: Toward an Expert on a Chip," *IEEE EXPERT*, Vol. 1, No. 3, pp. 55–62, August 1986.

[5] Watanabe, H., "VLSI Realization of Fuzzy Inference Mechanism," (in Japanese), *Trans.(Section A) of Institute of Electronics, Information and Communication Engineers*, Vol. J72-A, No. 2, pp. 179-187, February, 1989.

[6] Watanabe, H., W. Dettloff and E. Yount "A VLSI Fuzzy Logic Controller with Reconfigurable, Cascadable Architecture," *IEEE Journal of Solid–State Circuits*, Vol. 25, No. 2, pp. 376–382, April 1990.

[7] Watanabe, H., "VLSI for Fuzzy Inference," (in Japanese), pp. 46-56, in *Fuzzy Logic Applications*, edited by K. Hirota, Kogyo Chousa Kai (Industrial Research Association), February 1991, Tokyo.

[8] Watanabe, H., J. R. Symon, W. D. Dettloff and K. E. Yount ,"VLSI Fuzzy Chip and Inference Accelerator Board Systems," *Proc. of IEEE International Symposium on Multi–Valued Logic*, pp. 120–127, May 1991.

[9] Watanabe, H., "Some Consideration on Design of Fuzzy Information Processors — From a Computer Architectural Point of View," *Proc. of International Fuzzy Engineering Symposium '91*, pp. 387–398, November 1991.

[10] Watanabe, H., J. R. Symon, W. D. Dettloff and K. E. Yount, "Fuzzy VLSI Chip and Inference Accelerator Board System," pp. 211--243, in *Fuzzy Logic for the Management of Uncertainty*, edited by L. A. Zadeh and J. Kacprzyk, John Wiley & Sons, 1992, New York, NY.

[11] Watanabe, H., "A RISC Approach to Design of Fuzzy Processor Architecture," *Proc. of IEEE International Conference on Fuzzy Systems*, pp. 431–440, March 1992.

[12] Watanabe, H. and D. Chen, "Evaluation of a RISC Processor for Fuzzy Inference," pp. 429-432, *Proceedings of 8th Fuzzy Systems Symposium*, Hiroshima, Japan, May 1992.

[13] Watanabe, H. and D. Chen, "Evaluation of Fuzzy Instructions in a RISC Processor," pp. 521-526, *Proceedings of 2nd IEEE International Conference on Fuzzy Systems*, San Francisco, CA, March 1993.

[14] Watanabe, H., "Digital Hardware System — VLSI Fuzzy Inference System," (in Japanese), in *Introduction to Fuzzy Information Processing*, edited by K. Asai, *in press*, Ohmsha, Ltd., Tokyo.