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The Digital Fuzzy Inference System Using Neural Networks

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Abstract

Fuzzy inference system which inferences and processes the Fuzzy information is designed using digital voltage mode neural circuits. The digital fuzzification circuit is designed to MIN,MAX circuit using CMOS neural comparator. A new defuzzification method which uses the center of area of the resultant fuzzy set as a defuzzified output is suggested. The method of the center of area(C.O.A) search for a crisp value which is correspond to a half of the area enclosed with inferenced membership function. The center of area defuzzification circuit is proposed. It is a simple circuit without divider and multiflier. The proposed circuits are verified by implementing with conventional digital chips.

1. Introducton

To process fuzzy control and fuzzy decision making, the fuzzy circuits are proposed and implemented. Yamakawa[1] proposed fuzzy circuits and architecture of fuzzy computer. To implement fuzzy inference chip and fuzzy computer, the fuzzy circuit and fuzzy memory[2] are needed and classified into analog circuit and digital circuit. The analog circuits in opposition to digital circuits are weak to the noise and there is a problem of computer interfacing. According to input and output signals, the fuzzy circuit is classified into voltage mode and current mode. The current mode circuit is easy to implementing fuzzy circuit compare to the voltage mode circuit except the problem of fan-out.

2. The digital MIN,MAX circuits using neural networks

The MIN(MAX) counting is a basic computation for processing and inferencing of fuzzy information. The digital MIN(MAX) circuits are designed by using a neural comparator circuit. The neural comparator circuit is shown in Fig.1. The input data A and B are composed of 4 bit data. The output is decided after the input data A of PMOS is compared with the input data B of NMOS. The input bits have the same weight value (W/L) and neuron part consists of 2 CMOS inverters. The synaps are replaced by ON resistance of MOS transistor. If the PMOS transistor is conducted (ON state), VDD voltage appears at V(1) node. If the NMOS transistor is conducted, the voltage of V(1) node dropes to GND voltage. According to the number of conducted PMOS and NMOS, the analog output voltage between 0 v and 5 v is determined. The MIN(MAX) circuit which is necessary for fuzzy chip design is composed of a 4 bit neural CMOS comparator. Fig.2 shows 4 bit digital MIN circuit using CMOS neural comparator. The 4 bit MIN circuit is composed of neural comparator, an inverter, and a transmission gate. If the input data A is smaller than input data B, the output of comparator is low but the output of inverter passing through inverter is high and also output of next inverter is low thus, the PMOS of transmission gate is conducted. The output of MIN comes out the smaller value between 4 bit input data A and input data B. The Fig.3 shows to MAX circuit for 4 bit digital. The operation of MAX circuit is similar to MIN circuit.

3. The defuzzification circuit using the method of the center of area

The Fig.4 shows the block diagram of the proposed defuzzification circuit. The method of defuzzification utilizes the center of area (C.O.A). The center of area method searches for a crisp value which corresponds to a half of area enclosed with inferenced membership function. The defuzzification circuit using C.O.A method is proposed using ADD, RAM, P.C(program counter) and comparator circuit. The operation of defuzzification circuit is as follows: the upper ADD circuit seeks for the area by accumulating the inferenced data which is stored in RAM1. To seek for a half of area, the shift register shifts right by one bit. The lower ADD circuit seeks for the area by accumulating the inferenced data which is stored in RAM2. At the comparator, the value that is passing through a shift register is compared with the value of area which is searched by the lower ADD. If the value of a half of area is larger than the value obtained at lower ADD, the output of comparator is high and P.C. increases by one. The signal of P.C. is control signal. As the P.C. increases by one, the data in RAM2 goes to the lower ADD. On the other hand, if the value of a half of area is smaller than the value of area calculating to ADD of lower part, the output of comparator is low. Consequently, the address of P.C. does not increase. the value of area at lower ADD does not increase but the upper ADD accumulates the data by continuing external clock signal. The comparison to the value of a half of area and the value of area is repeated. When the value of a half of area come out, this action is halted. The number address of P.C. is a crisp value which corresponds to a half of the area enclosed with inferenced membership function. The performance of this method is comparable to the method of center of gravity which is widely used. The advantage of the proposed method is that it can be implemented without divider and multiplier.

4. Fuzzy inference system

The Fig.5 shows the block diagram of a fuzzification circuit. This block can process the 7 fuzzy rules. The rule and input data are composed of 4 bit data. The proposed MIN(MAX) circuit is made of a comparator, inverters and tranmission gate. The Fig.4 shows the block diagram of a proposed defuzzification circuit. The Fig.6 shows the fuzzy inference system.

5. The comparison of defuzzification method

There are number of defuzzification methods used for transforming a fuzzy membership function into a crisp value in fuzzy control. These methods are maximum, mean of maximum, and center of gravity, etc. The method of center of gravity is widely used in engineering application. But for the shape of convexity and interval for inferenced fuzzy membership function, a problem happens to in inadequatness for robot controlled command[3]. To compare the performance of C.O.G. with C.O.A., Method is applied to the binarization of FAX image. The Fig.7 shows the binarization of character image using threshold value obtained by C.O.G. defuzzification. The Fig.8 shows the binarization of FAX image using C.O.A. defuzzification method. Even though the widely used C.O.G. method performs better than C.O.A. method, depending on the rules provided, the C.O.A. method performs almost equivalent to C.O.G. method.

6. Conclusion

The new fuzzy circuits(MIN, MAX) are designed by a neural CMOS 4 bit comparator, inverter and transmission gate. In this paper, a new defuzzification method which uses the center of the area(C.O.A.) of the resultant fuzzy set as a defuzzified output is suggested. A C.O.A. defuzzification circuit is proposed without a divider and a multiplier. The proposed circuits are verified by implementing with conventional digital chips. The fuzzy inference is applied to image segmentation and binarization of FAX image.

References

[1] T. Yamakawa, "Intrinsic fuzzy electronic circuits for sixth generation computer", Fuzzy computing, North-Holland, pp. 157-171. 1988.

[2] K. Hirota and K. Ozawa, "The concept of fuzzy Flip-Flop", IEEE Trans. on System, Man and Cybernetics, vol. 19, no. 5. pp. 980-997 1989.

[3] N. Pfluger, J. Yen and R. Langari, "A defuzzification strategy for a fuzzy logic controller employing prohibitive information in command formulation", IEEE International Conference on fuzzy systems, vol. 1, pp. 717-723, May 1992.

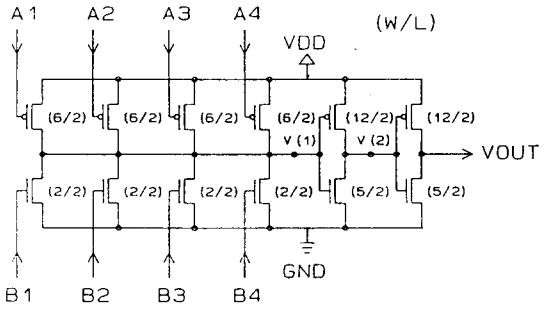

Fig.1 The 4 bit comparator using neural circuit

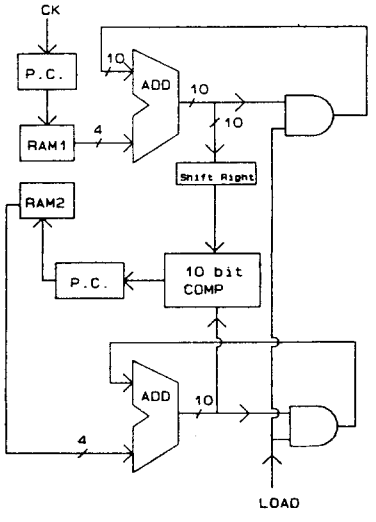

Fig.4 The block diagram of a defuzzification circuit

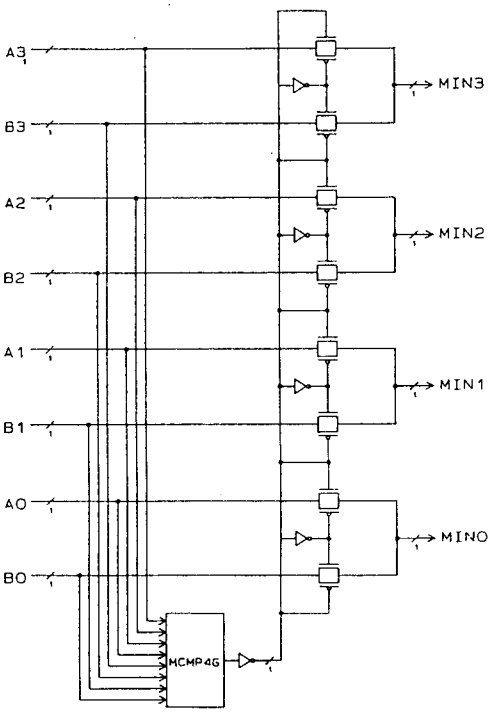

Fig.2 The 4 bit digital MIN circuit

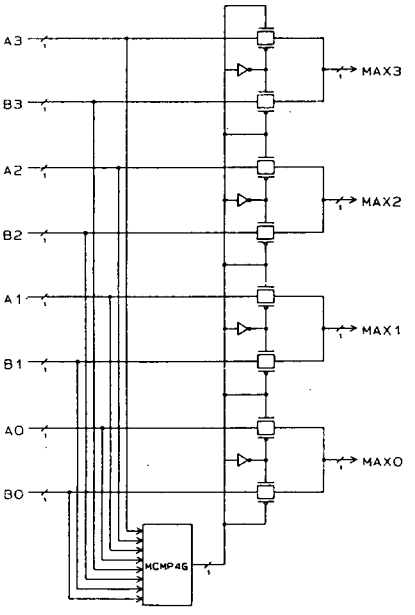

Fig.3 The 4 bit digiatl MAX circuit

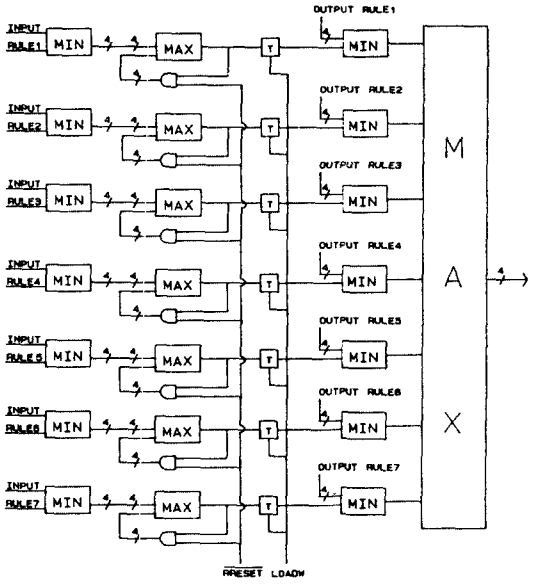

Fig.5 The block diagram of a fuzzification circuit

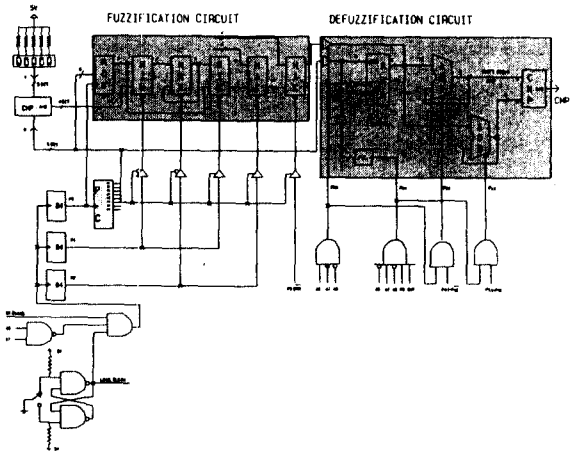

Fig.6 The fuzzy inference system

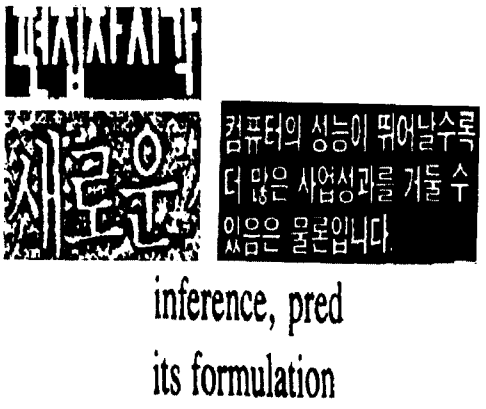

Fig.8 The binarization by the C.O.A defuzzification method

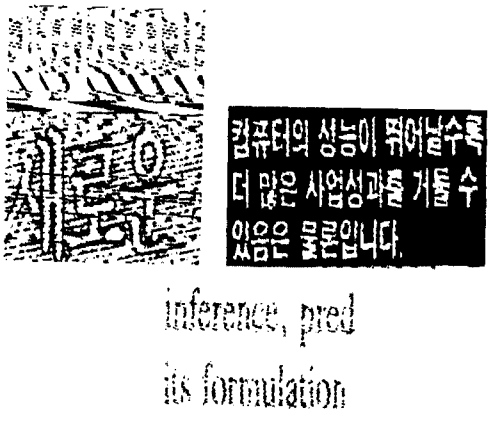

Fig.7 The binarization by the C.O.G defuzzification method