FUZZY FLIP-FLOP CIRCUIT AND ITS APPLICATION

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ABSTRACT

In this paper the characteristics of the fuzzy flip-flop which was proposed as a fuzzy sequential circuit is firstly mentioned. Secondly the circuit construction of typical fuzzy flip-flop circuits using VHDL(Very high speed integrated circuit Hardware Description Language) compiler and simulator is presented. Finally the possibility of the application of the fuzzy sequential circuit will be mentioned.

1.INTRODUCTION

The application of the fuzzy set theory and fuzzy logic have been increased and widely used in variety fields. Some application fields, where the real time processing of the fuzzy inference or economizing the equipment of fuzzy control system is needed, require the fuzzy hardware system. In order to meet these demands, fuzzy hardware systems have been studied and commercialized under the name of "fuzzy chip" or so called "fuzzy computer". However these ordinary fuzzy hardware system can only process the single stage fuzzy inference because of not having the fuzzy memory modules.

The ordinary fuzzy hardware system, especially using digital technique, is constructed by the fuzzy gate circuits (fuzzy negation gate, t-norm gate, and s-norm(t-conorm) gate) and static Random Access Memory to store the fuzzy production rules and membership functions. In other words the fuzzy hardware system is constructed as a fuzzy combinational circuit. It is difficult for the ordinary fuzzy hardware system to apply to the multi stage fuzzy inference or the flexible fuzzy inference jobs. In the case of an ordinary binary computer, combinational circuits and sequential circuits are used efficiently. The concept of fuzzy sequential circuits will be essentially necessary for fuzzy hardware system.

This paper firstly mentions the definition and characteristics of the 4 types fuzzy flip-flop circuits as the fuzzy sequential circuit. All of these types are extension forms to the fuzzy

logic from the binary logic including their basic 4 characteristics (i.e. memory or hold, set, reset, and inversion). Secondly this paper mentions the circuit design and its characteristics using VHDL (Very high speed integrated circuit Hardware Description Language) compiler and logic simulator. Finally we mention the application of the fuzzy flip-flop circuit.

2. DEFINITION OF THE FUZZY FLIP-FLOP

The fuzzy flip-flop has been defined and introduced as an extended form of that of binary J-K flip-flop using the concepts of fuzzy negation, t-norm, and s-norm operation[1]. Definitions of basic four types of fuzzy flip-flop's which are min-max type, algebraic type, bounded reset type, and bounded set type are shown in the following equations (2-1)～(2-4),

(1) min-max type
$$Q(t)=\{J\vee(1-K)\}\wedge(J\vee Q)\wedge\{(1-K)\vee(1-Q)\}, \quad (2-1)$$
(2) algebraic type
$$Q(t)=J + Q - JQ - KQ, \quad (2-2)$$
(3) bounded reset type
$$Q(t)=1\wedge\{0\vee(J-Q) + 0\vee(Q-K)\}, \quad (2-3)$$
(4) bounded set type
$$Q(t)=0\vee\{1\wedge(J+Q) + 1\wedge(2-K-Q) - 1\}, \quad (2-4)$$

, where the variable t-1 is omitted in the right hand side of equation (2-1)～ (2-4). Detailed characteristics of these fuzzy flip-flop's have been analyzed in references[2] [3]. Each of these fuzzy flip-flop's includes four basic characteristics which are memory of fuzzy

information (J=K=0), output of the inverse fuzzy information (J=K=1), set (J=1, K=0), and reset (J=0, K=1) the fuzzy information.

3. VLSI DESIGN OF THE MIN-MAX TYPE FUZZY FLIP-FLOP CIRCUIT

In this section, for example, a VLSI design of min-max type fuzzy flip-flop as the lower cell of the fuzzy sequential circuit is presented. VLSI source of min-max type fuzzy flip-flop is designed using VHDL, and optimization of the circuit is used VHDL compiler and simulator (by Synopsys Inc.). List 3.1 shows the VHDL source code of the min-max type fuzzy flip-flop. The fuzzy information each of which is expressed by 4 bit are processed in parallel. It is defined as "UNSIGNED (3 downto 0)" in the "entity" block in the list. "Architecture" block in the list describes the operation of min-max type fuzzy flip-flop. All of these function in the "process" block is synchronously processed with clock pulse (CLK). Fig. 3.1 shows the circuit diagram, designed by VHDL compiler, of the min-max type fuzzy flip-flop. This diagram is optimized under the condition of the smallest area of the VLSI. The main element of the circuit is 4 bit magnitude comparator, the others are D-type flip-flop and basic gate circuits. Table 3.1 shows the area information of the circuit, and Table 3.2 shows the delay information. The area of the circuit is 223.0 which is the relative value when area of NOT gate is equal to 1.0.

The time unit of the delay information is n sec.

On the other hand, under the condition of the fastest delay time, min-max type fuzzy flip-flop circuit is also able to design. In this case the main units of the circuit will be multiplexor and 4 bit magnitude comparator. The total area, in this case was 294.0. The area was increased by 1.32 times that of the previous smallest condition. However delay times of the rise and fall edge were improved as 1.96 n sec and 1.68 n sec respectively.

The simulation was done following "TEST BENCH" program described by VHDL using the VHDL simulator. In the "TEST BENCH" program, J = "0000" and K = "1111" were firstly fed to the fuzzy flip-flop, i.e. to reset the fuzzy flip-flop, then the analysis will start. Clock cycle is 20 n sec. Close agreement between simulated and calculated values was obtained in all cases.

Table 3.1 Area information of the circuit.

Attributes: n - noncombinational
s - synthetic module
h - hierarchical

Reference	Library	Unit Area	Count	Total Area	Attributes
A02	class	2.00	20	40.00	
FD1	class	7.00	8	56.00	n
IV	class	1.00	19	19.00	
IVA	class	1.00	2	2.00	
MINMAX_cmp_0		16.00	1	16.00	s, h
MINMAX_cmp_1		17.00	1	17.00	s, h
MINMAX_cmp_2		17.00	1	17.00	s, h
MINMAX_cmp_3		16.00	1	16.00	s, h
MINMAX_cmp_4		16.00	1	16.00	s, h
MINMAX_sub_0		4.00	1	4.00	s, h
MINMAX_sub_1		4.00	1	4.00	s, h
MINMAX_sub_2		4.00	1	4.00	s, h
MINMAX_sub_3		4.00	1	4.00	s, h
MINMAX_sub_4		4.00	1	4.00	s, h
MINMAX_sub_5		4.00	1	4.00	s, h

Total 15 references 223.00

List 3.1 VHDL source code of min-max type fuzzy flip-flop circuit.

```
entity MINMAX is
        port( CLK: in BIT;
                J.K: in UNSIGNED(3 downto 0);
                Q.QN: buffer UNSIGNED (3 downto 0));
end MINMAX1;

architecture BEHAVIOR of MINMAX is
begin
        process
        variable U1.U2.U3.U4.U5.U6: UNSIGNED (3 downto 0);
        begin
                wait until CLK'event and CLK='1';
                U4 := "1111" - K;
                if( J > U4 ) then
                        U1:= J;
                else
                        U1:="1111" - K;
                end if;

                if( J > Q ) then
                        U2:= J;
                else
                        U2:= Q;
                end if;
                U5:="1111"-K;
                U6:="1111"-Q;
                if( U5 > U6 ) then
                        U3:= "1111"-K;
                else
                        U3:= "1111"-Q;
                end if;
                if( U1 < U2 ) then
                        if( U1 < U3) then
                                Q<=U1;
                        else
                                Q<=U3;
                        end if;
                else
                        if( U2 < U3 ) then
                                Q<=U2;
                        else
                                Q<=U3;
                        end if;
                end if;
                QN<="1111"-Q;

        end process;
end BEHAVIOR;
```
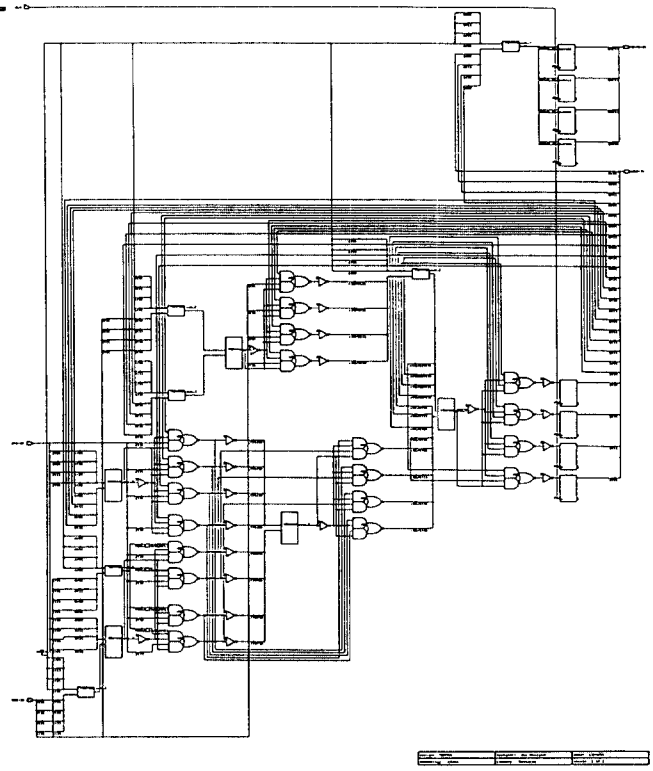

Fig. 3.1 Circuit diagram of the min-max type fuzzy flip-flop.

Table 3.2 Delay time information of the circuit.

Point	Type	Fanout	Max Delay rise	Max Delay fall	Min Delay rise	Min Delay fall
Q[3]	out	6	2.26	1.79	2.26	1.79
Q[1]	out	6	2.11	1.74	2.11	1.74
Q[2]	out	6	2.11	1.74	2.11	1.74
Q[0]	out	6	1.96	1.68	1.96	1.68
QN[0]	out	1	1.09	1.37	1.09	1.37
QN[1]	out	1	1.09	1.37	1.09	1.37
QN[2]	out	1	1.09	1.37	1.09	1.37
QN[3]	out	1	1.09	1.37	1.09	1.37

4. VLSI DESIGN OF THE FUZZY REGISTER

In this section, VLSI of the fuzzy register circuit is designed. Based on the VHDL source of the fuzzy register circuits, VLSI of the fuzzy register circuit is designed as shown in Fig. 4.1. Here fuzzy register is designed by using four fuzzy flip-flop circuits in order to simplify the circuit diagram. Here membership information and inputs J and K, and outputs Q are digitized by {0000, 0001, ... ,1111}, respectively. MEN1, MEN2, MEN3, MEN4 are inputs of the membership value to the circuit and CLK is the clock pulse input. In case of the total number of fuzzy flip-flop's used are eleven to take into consideration the practical use. The total area is 2546.0. The fuzzy flip-flop (min-max type) as fundamental units of fuzzy register accounts for 96.3 percent of all area of the circuit. Remaining 0.7 percent is fundamental binary gate circuits for the control pulse selection. In this case, delay time information of present fuzzy register circuit. Max delay time is 2.26 n sec and 1.79 at rise and fall, respectively. In this section we used the min-max type fuzzy flip-flop as the fundamental unit of the fuzzy register, as a matter of course it can realize using
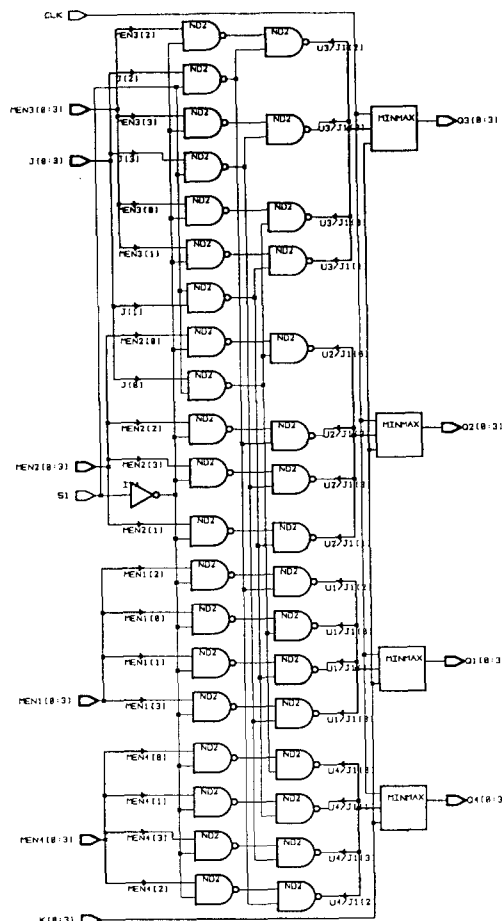

Fig. 4.1 Circuit diagram of the fuzzy register circuit.

5. CONCLUSION

The fuzzy flip-flop which was proposed as a fuzzy sequential circuit is firstly mentioned. Secondly the circuit construction of the typical fuzzy flip-flop using VHDL compiler and simulator is presented. Finally fuzzy register circuit as the application for the fuzzy sequential circuit was mentioned.

REFERENCES
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