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Analogue-Digital Hybrid Circuit for an Adaptive Fuzzy Network

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ABSTRACT

This paper describes a fuzzy network circuit of analogue and digital mixed operation. The circuits are suggested for membership function, MIN function and normalization function using either linear voltage-controlled MOSFET resistance or pulse stream operation. The analogue-digital hybrid fuzzy hardware is extensible to the fuzzy-neural network as its basic configurations are already used in URAN-I of 135,424 synaptic connections.

I. INTRODUCTION

Fuzzy controllers have recently illustrated practical applications in various areas. The fuzzy system is realized by a use of conventional digital computers or a special fuzzy processor. In general, High speed fuzzy processors has been expected for the complex and real-time control system. With the extensibility to the neural network, fuzzy hardware devices can yield the substantial improvement on the application domains. In this paper, the new analogue MOSFET membership function circuit is described for the fully adaptable VLSI fuzzy device implementation. The structure for both of the analogue and digital is considered for its wide application as well as its simple operation. Inputs of voltages or voltage pulses are used to signal through membership function circuit of premise part and consequence part of fuzzy or fuzzy-neural network.

The same basic configuration has been already used in implementing the neural network hardware of analogue-digital mixed operation. URAN(Universally Reconstructable Artificial Neural-network) of 135,424 connections is recently developed using the MOSFET voltage-controlled linear resistance and pulse-based operation. And the fuzzy inference machine and the neural network can be efficiently integrated in the same device or system.

II. FUZZY LOGIC SYSTEM OF HYBRID CIRCUIT

The fuzzy logic control system is based on fuzzy inference as in Fig. 1. It can be also described as the block diagram in Fig. 2. In this paper, new analogue-digital hybrid circuits are suggested for each block of Fig.2 using pulse operations and linearized MOSFET resistances. Although variety of inputs can be applied, only the input of voltage level is mentioned for its simple convertibility to pulses.

Adaptable Membership Function of Analogue-Digital Hybrid Circuit

There have been reported various membership function circuits on the analogue operation. Also there are several digital hardwares of pulse train, the new adaptable membership function presented in this paper is using the simple configuration as well as the small number of transistors, with the

improved accuracy. The whole fuzzy controller or fuzzy-neural network can be implemented without the complex analogue component, thereby permitting the fabrication using the standard, low-cost digital CMOS process. The basic concept of unit element over the whole fuzzy or neural hardware is come from the programmable, linear and bipolar current source.

The current-voltage(I-V) relationship of MOSFET in the triode region could be clearly adopted to code the multiplication, a membership function, a neural synaptic weight and state respectively. The equation of interest is that for the drain-source current I_{DS} for a MOSFET in linear or triode region : -

$$I_{DS} = \frac{\mu C_{ox} W}{L} [(V_{GS} - V_T)\cdot V_{DS} - \frac{V_{DS}^2}{2}]$$

Here, C_{ox} is the oxide capacitance/area, μ the carrier mobility, W the transistor gate width, L transistor gate length, and V_{GS}, V_T, V_{DS}, the transistor gate-source, threshold and drain-source voltage respectively. This expression for I_{DS} contain a useful product term : - (μC_{ox} W/L) V_{GS} V_{DS} -. However, it also contains two other terms in $V_{DS}\cdot V_T$ and V_{DS}^2. Though one may ignore this imperfection in the arithmetic, it is chosen rather, to remove unwanted terms via the balanced voltage to a MOSFET with the symmetric current sensing element - MOSFET of gate-to-drain connected for example. And the sensed current I_S yields as in the following : -

$$I_S = k [(V(T_{ij}) + V' - V_T)\cdot(2V') - 2V'^2]$$
$$= k (V(T_{ij}) - V_T)\cdot(2V')$$

$$\text{where} \quad k = \frac{\mu C_{ox} W}{L}$$

Hence the out current I_{out} with the mirrored current and biased offset current can be made as

$$I_{out} = k' [V_{GS} - V_{offset}]$$

This is a fairly well-known relationship, and can tailor the arbitrary membership function and values also constitute an electronic neural synapse. The idea is based on the former ' MOSFET voltage-controlled linear resistance ' for use in signal processing such as filters. Two transistors are used for the current sensing to form the current mirror with the one, while the other one keeps the balanced condition of main transistor in triode region. With the other additional transistor of externally-controlled current source at output, the offset term is compensated and the opposite polarity of linear programmable current is attained. The reference voltage V_{WEIGHT} of the coefficient should be kept the main transistor in the linear region. This is not a difficult constraint to satisfy. The attraction of this cell is that active elements such as operational amplifiers are not necessary, and can provide full wired-OR capability to generate adaptable and reconstructable custom functions such as membership functions. The CMOS test cell is made up with the size of 45μm x 45μm in 1.2μm standard CMOS technology of double-metal-single-poly. One general membership function defined by 4-point can be implemented with 6 cells in an equivalent chip area as shown in Fig. 3, with the experimental cell characteristics of Fig. 4. It is around 110μm X 110μm in size of VLSI chip area. The accuracy of one basic cell is 8-bit from the experimental result of test chip in and the slope of membership function can be easily changed with the external reference voltages. Various membership function shapes can be generated by 'WIRED-OR' as each unit acts as the controlled current source.

MIN Function and Normalization Function

With current outputs from membership function, the MIN function can be attained as in Fig. 5. Each current output from membership function is converted to the pulse width, which is inverted and applied to NOR relatively. The output of NOR

is the minimum pulse width from inputs, equivalently. With the aid of pulse operation, the MIN function can be easily
implemented with the pulse-width output. Those MIN outs of pulse width is directly used to switch the voltage-controlled linear current source as illustrated in Fig. 6, exactly similar to the synapse operation in URAN. The output of weighted summation is produced in the form of voltage at the capacitor. For the normalization, every MIN output current is also summed at the capacitor, which is used to change the current amount Q. Assuming three MIN output T1, T2, T3 with the block of Fig. 7, the final output TO becomes as required in normalization : -

$$TO = \frac{W1 \cdot T1 + W2 \cdot T2 + W3 \cdot T3}{k \cdot (T1 + T2 + T3)}$$

where $Q = k \cdot (T1+T2+T3)$ and k is the controlling coefficient of MOSFET resistance. TO is in the form of pulses and can be easily interfaced both the analogue and digital system.

Integration with Hybrid Neural Network

The idea of the membership function, MIN function, normalization function is based on the discrete or digital pulse input/processing and continuous or analogue bipolar current generation/wired-OR. And it is also used to build the consequent part of fuzzy-neural network because of its inherent capability of tunable multiplication. There is the other test-chip using the basic cell to build high speed and huge density of neural network of adaptable 135,000 connections per chip. With the proposed hybrid circuit of programmable linear element, the speed of fuzzy operation is less than 10μs per with 6 bit input/output and 15 MHz system clock. There is almost no constraint in numbers of input and output with the parallel construction of basic unit due to its inherent analogue wired-OR of digital processing.

III. Conclusion

One of distinct analogue circuitry with digital processing has been described. There are also reported several different types of pulse operated circuit. None has yet been used to configure an adaptive fuzzy network or an adaptable membership function but this is now being done. Current estimates for the numbers of fuzzy network implementable using this technique would be around 64 inputs of 8 group of membership function with 32 outputs, using 8mm x 8mm die as an example.
In addition it is now expected to develop the similar techniques to consturct fuzzy neural network system with the same circuit design and the same operation principle.

IV. REFERENCES

[1] O. Ishizuka et al, "Design of Fuzzy Controller with Normalization Circuit," ICFS, pp1303-pp1308, 1992

[2] Il Song Han and Ki Hwan Ahn, "Neural Network VLSI Chip Implementation of Analog-Digital Mixed Operation for more than 100,000 Connections," Micro-Neuro'93, pp159-pp162, 1993

[3] Il Song Han, "Analog Circuit for Neural Network," ICANN'91, Vol.2, pp. 1577-1579, 1991

[4] H. Watanabe, "Hardware Approaches to Fuzzy Logic Applications," IEEE FUZZ'93, Tutorial #7, 1993

Fig. 1. Fuzzy Logic System

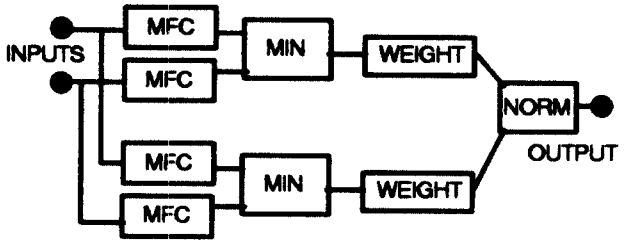

Fig. 2. Circuit Blocks of Fuzzy System

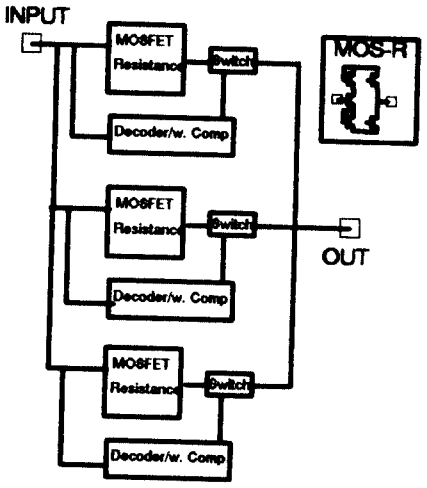

Fig. 3. Membership Function Circuit and Configuration

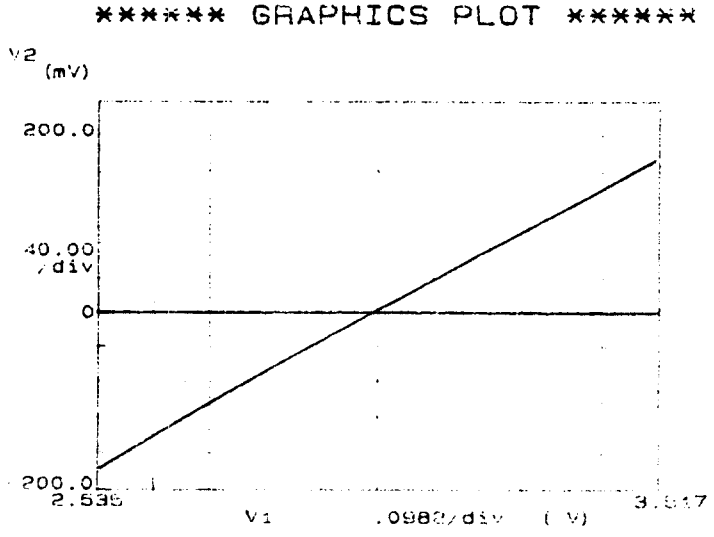

Fig. 4. Electrical Characteristic of VLSI Cell

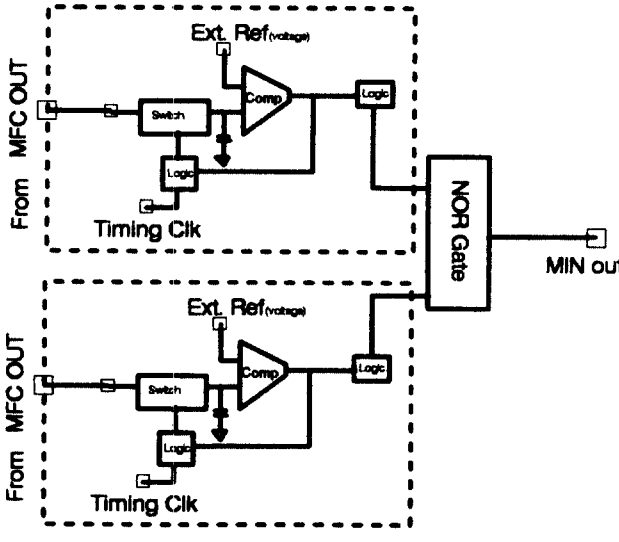

Fig. 5. MIN Function Circuit Block

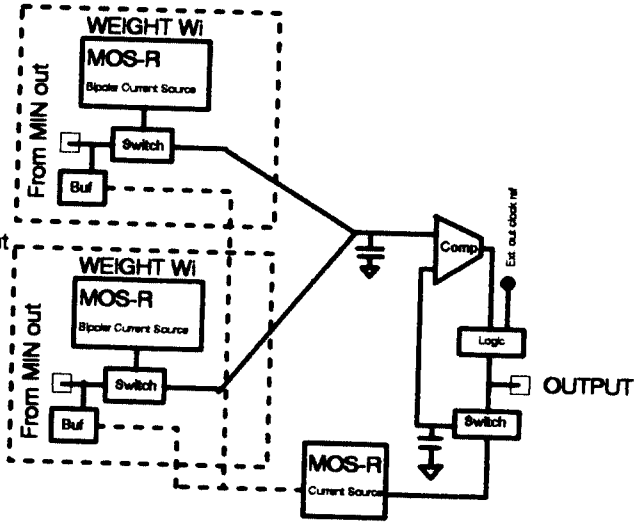

Fig. 6. Normalization Circuit Block