Fifth IFSA World Congress (1993), 785 - 788

Current Mirror-Based Approach to the Integration of CMOS Fuzzy Logic Functions

Marek J. Patyra[1], Laurent Lemaitre[2], and Daniel Mlynek[2]

[1] Department of Computer Engineering, University of Minnesota, Duluth, MN 55811, USA
[2] Swiss Federal Institute of Technology (EPFL), 1015 Lausanne, Switzerland

ABSTRCT: This paper presents the prototype framework for automated integration of CMOS current-mode fuzzy logic circuits using an intelligent module approach. The library of modules representing the standard fuzzy logic operators was built. These modules were finally used to synthesized sophisticated fuzzy logic units. Fuzzy unit designs were made based upon the results of a newel methodology of the current mirror-based fuzzy logic function synthesis. This methodology is actually incorporated into the presented framework. As an example, the membership function unit was synthesized, simulated, and the final layout was generated using the presented framework. Finally, the fuzzy logic controller unit (FLC) was generated using the proposed framework. Simulation as well as measurement results show unquestionable advantages of the proposed fuzzy logic function integration system over the classical design methodology with respect to the area, relative error and performance.

1. INTRODUCTION

The recent explosion of interest in consumer products based on fuzzy logic technology indicates a need for a new generation of microchips. Some analog and digital solutions leading to VLSI implementation of fuzzy units have been proposed during the last eight years. In this paper, we focus on the analog, current-mode implementation of fuzzy logic circuits. Therefore, the use of current mirrors as fuzzy logic building blocks perfectly matches this design technique, however it requires a complete overhaul of classical VLSI circuit design philosophy. That fact stimulated the presented work, where, a new strategy for CMOS implementation of fuzzy logic units is proposed.

2. NOTION OF FUZZY NUMBERS

One of the method for representing the real number x ranging between 0 and n can be provided by the following expression:

$$x = \mu_1 + \ldots + \mu_i + \ldots + \mu_n \qquad \text{(EQ 1)}$$

where μ_i belongs to the interval [0,1], and satisfies: $\mu_i = 1$ when $x \geq i$. On the other hand, the sequence $[\mu_i]_{i=1+n}$ may be called the fuzzy number corresponding to x (coefficient μ_i is the ith fuzzy unit of the real x) [5]. When x is natural, all the μ_i equal to either 0 or 1 and correspond to the "Boolean thermometer code" of x. For example, let's take the following set of parameters: n=4, x_1=3 and x_2=3.2, then the fuzzy numbers of x_1 and x_2 can be represented by: $FIT_1 = 0111$ (in fact: x_1=0+1+1+1=3), and FIT_2=0.2111 (also: x_2=0.2+1+1+1=3.2), respectively.

As an example, the expression of the membership function of a variable x toward a crisp value i reduces to:

$$MF(x, i) = \mu_i \wedge \overline{\mu_{i+1}} = MAX(0, MIN(1 - |x - 1|)) \qquad \text{(EQ 2)}$$

Figure 2 shows the triangular shape of MF for $i = 2$ and $n = 5$. As can be seen, the proposed method leads to the consistent definition of the fuzzy number. The MF has been synthesized using the operators: $\neg$, **P**, and **N**, which are defined in the next section.

3. ELECTRICAL REPRESENTATIONS

The most commonly used fuzzy operators MAX and MIN (s-norm and t-norm, respectively) cannot be directly replaced by electrical circuits. In order to reduce the complexity of electrical realization of general fuzzy functions three "primitive" operators denoted by the symbols: $\neg$, **P**, and **N** are introduced. There are as follows:

Duality operator $\neg$:

$$\neg X = -X \qquad \text{(EQ 3)}$$

Positive-cut operator **P**:

$$P(X) = \begin{bmatrix} -X if (X \geq 0) \\ 0 otherwise \end{bmatrix} \qquad \text{(EQ 4)}$$

Negative-cut operator **N**:

$$N(X) = \begin{bmatrix} -X if (X \leq 0) \\ 0 otherwise \end{bmatrix} \qquad \text{(EQ 5)}$$

All fuzzy logic propositions can be formulated as an additive combination of the primitive operators $\neg$, **P** and **N**. For instance, the following relations are straightforward:

$$X \vee Y = \text{MAX}(X,Y) = \text{N}(Y + \neg X) + Y \qquad \text{(EQ 6)}$$

$$X \wedge Y = \text{MIN}(X,Y) = \text{P}(Y + \neg X) + Y \qquad \text{(EQ 7)}$$

$$\bar{X} = \text{NOT}(X) = 1 + \neg X \qquad \text{(EQ 8)}$$

Special properties of $\neg$, **P** and **N** help to obtain reduced forms of compositional expressions. As described in [5] and

depicted in Figure 1, the electrical implementations of **P** and **N** operators are simple and they can be represented by means of p and n CMOS current mirrors. In such an representation, the algebraic sum reduces to a simple electrical connection of wires.

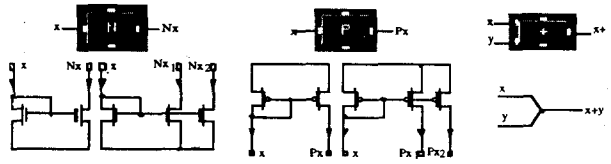

Figure 1 Symbolic representation of the primitive operators: positive-cut, negative-cut, and algebraic sum and their corresponding CMOS current mirror equivalents.

Let us again take the membership function described by (EQ 2) as an example. Figure 2 gives the optimized schematic that represents the membership function *MF* given by (EQ 2). The schematic resulting from the reduced form of *MF* (in terms of the primitive operators: ¬, **P** and **N**) is shown in the upper part of the captured screen (Figure 2). Applying relations given by (EQ 6) to (EQ 8) finally, we have a minimized equation describing *MF*, which can simply be transformed into a circuit representation:

$$MF(x, i) = N(Ax + \neg 1) \qquad \text{(EQ 9)}$$

where:

$$Ax = P[P(Nx + i) + P(Ni + x) + \neg 1] \qquad \text{(EQ 10)}$$

In order to verify the proposed approach to fuzzy logic function synthesis we developed a fuzzy logic simulation environment (FLSE) utilizing the HP software package VEE-Test [8]. The results of synthesis and simulation of the membership function circuit using FLSE are shown in Figure 2.

Having such a powerful tool like FLSE available, the next step toward the integration of CMOS fuzzy logic functions was to synthesize these functions using subcircuits representing introduced fuzzy operators.

4. CURRENT MIRROR-BASED FUZZY LOGIC CIRCUIT SYNTHESIS

As was previously shown, any class of a circuits performing fuzzy logic operations can be synthesized by means of simple current mirrors [9]. The hand crafted fuzzy logic cells for most of the principle operators were designed and published [10], but no automatization has been done so far in this field.

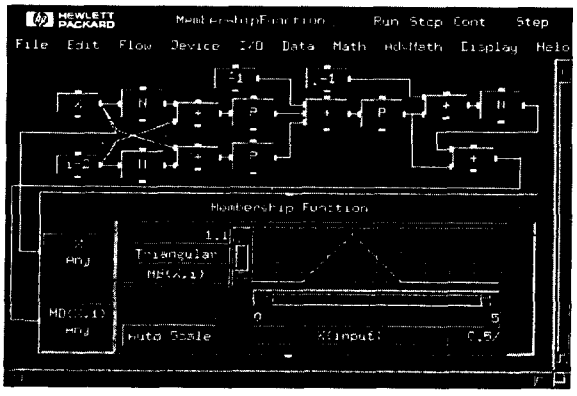

Figure 2 Structure of a triangular membership function and the corresponding logic-level simulation.

Our research goal was to fill this gap by introducing intelligent design system oriented on current mode implementation of fuzzy logic circuits. In analyzing the drawbacks of a classic, trivial approach, we found that the current mirror configuration involving current flow from p-mirror to two or more different n-current mirrors (connected to a single node), one of which being be open to the p-mirror current, and the other remaining closed, causes functional problems and should be forbidden for this class of applications. In such a configuration, current flow through the diode connected transistor (for the open n-current mirror) increases the drain-source voltage proportionally with the current density. On the other hand, the transistor of the cut-off n-current mirror remaining closed starts to pass current due to the increased drain-source voltage, which passes its saturation voltage. As a result, the high (up to 30% of the original current forced by p-current mirror) current flows through the undesired branch, destroying the originally designed current distribution in an analyzed structure. This fact causes the malfunction (due to the high error) of any circuits performing fuzzy operation which are built accommodating the analyzed above circuit structure.

In order to overcome this obvious disadvantage, present in more primitive designs of current-mode fuzzy logic circuits, the proposed methodology used for our synthesis purposes utilizes proper circuit structures. As a result, up to 50% of the overall structure can be minimized using the developed fuzzy logic function strategy described thoroughly in [6].

5. FRAMEWORK FOR AUTOMATED DESIGN OF FUZZY LOGIC CIRCUITS

We started to work out the framework idea with the concept of a limited hierarchy system, which means that we treated a basic current mirror circuit as a generic cell for building more complicated fuzzy structures like elementary fuzzy functions (MIN, MAX, etc.). As a result, cells representing these elementary fuzzy functions may then be assembled into a sophisticated fuzzy units. Hence, the hierarchy has only three stages: basic current mirror level, elementary fuzzy function level and fuzzy unit level. For instance, the fuzzy unit in this approach may represent a whole controller structure or its functional part like membership function unit, fuzzification unit, inference unit, or defuzzification unit.

The technical part of our framework involves a three-level intelligent generator system able to automatically choose the structure and generate the layout for each level separately. This also may be done hierarchically for the function or unit levels, depending on the requirements. The system was built using the L and Lx languages provided by the GDT Designer [3] from Mentor Graphics. This platform has been selected as a implementation vehicle for our framework due to its flexibility, programmability and portability in creating circuit generators. The basic principles of the generator system can be summarized as follows:

• *Long and short range symmetry. The short range symmetry refers to the symmetry at the elementary fuzzy function level The generic fuzzy function cell is optimized with respect to a short range symmetry. The fuzzy unit, built of several fuzzy*

functions, should also reflect the long range symmetry. In such a case, the long range symmetry requirement overrides the short range one. As a result, the simple building elements (current mirrors) are considered to be the basic building block of the total long-range symmetric unit structure.

- *Substrate and well contact compacting. The well and substrate contacts compacting is also ruled by the long range symmetry.*
- *Symmetrization of a global wiring. The requirement for the long term symmetry also involves the symmetrization of a wiring including the wiring within the cells representing elementary fuzzy functions.*
- *Merging of interconnections in the channel. The intelligent generator at the level of a unit is capable of merging the redundant interconnections within the channel. This involves modification of the generators at the level of an elementary functions.*
- *Shuffling of basic current mirror cells in order to obtain a global symmetry. The basic approach to long range symmetry lies in shuffling simple current mirrors at the level of the unit generator. An example of an obtained layout featuring this characteristic is discussed in the next section*
- *Portability - independence on the technology. The generators produced by our system use abstract knowledge extracted from a technology file, which, on the other hand, contains a quantitative representation of technology -related parameters (i.e. design rules, technological parameters etc.).*

Some of above mentioned characteristics may already be found in the existing analog CAD systems, e.g. [1] or [2], but others (restructuring the unit by the hierarchical modifications down to the level of basic cells) are unique for this domain. The system comprises four basic stages: generators for current mirrors, which are used as elementary blocks to build the library of basic fuzzy functions (MIN, MAX, BD, AD, and COM), the fuzzy unit synthesizer, which takes the description of the fuzzy function and decomposes&synthesizes it according to the structures of available fuzzy functions. After the decomposition and the synthesize of the unit structure, the information about the structure of the designed unit serves as the input set for the unit generator which generates a layout and performs all layout modifications described above down to the lowest level of hierarchy.

6. COMPARATIVE EXAMPLE

The following comparative example was performed in order to verify the invented idea and prove the usefulness of the proposed system. First the membership function circuit was designed using the classical approach, which starts from the analytical function of a considered circuit:

$$MF = MAX\{I0, MIN(I1, AD[ALPHA, BD(X, VP)])\} \quad (EQ\ 11)$$

This representation can be rewritten in the current domain as follows:

$$IMF = MAX\{I0, MIN(I1, AD[IALPHA, BD(IX, IVP)])\} \quad (EQ\ 12)$$

The IVP current represents the central value, I0 minimum, and I1 maximum current levels respectively. Current IALPHA provides a current shift. The current-mode implementation of subcircuits MIN, MAX BD and AD can be found, for instance in [7], [9] or in [10]. This kind of trivial approach consists of simple connection of listed subcircuits to form a function structure described by (EQ 2).

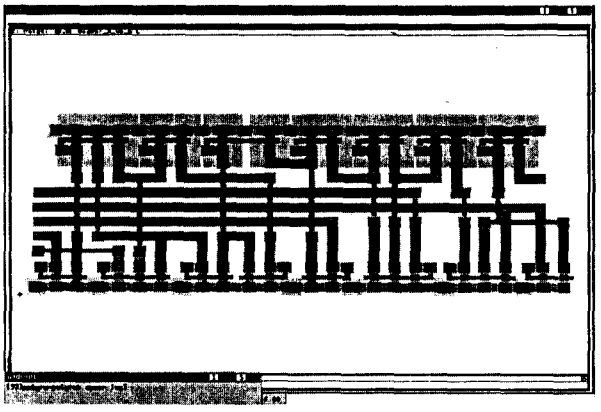

Figure 3 Classically generated layout for the membership function (MF) circuit.

Then, the layout generator was manually written in L language [3] using a typical approach recommended by Mentor Graphics manuals. The appropriate layout is shown in Figure 3. The upper row contains p transistors and the VDD rail; the bottom row contains n transistors and the GND rail. Interconnections occupy the channel in between these rows. The circuit schematic was extracted from the layout and simulated using the HSPICE [4]. Figure 4 shows the resulting graphs for this case. The I(RL) current represents the simulated membership function current, while MEMFUN(X) represents the theoretical membership function current. As can be seen from Figure 4, the average relative error between theoretical and simulated characteristics is typically about 25%.

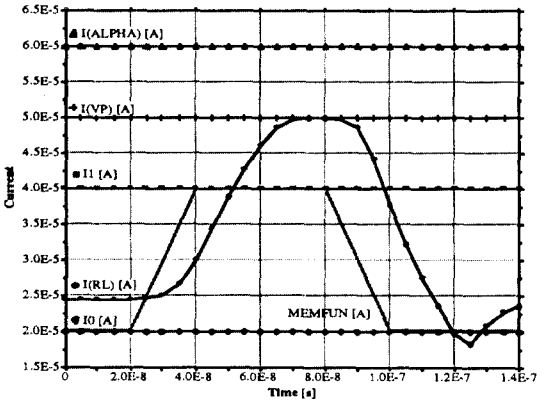

Figure 4 Results of HSPICE simulation of the analyzed membership function (MF) circuit.

For comparison, the membership function unit was synthesized using the presented framework, extracted and simulated using HSPICE, and the final layout for the unit was generated (see Figure 5). The layout topography is similar to that of Figure 3 (p transistors in the upper row, n transistors in the bottom row). The formula for the applied membership function was exactly the same as used in the previous example. However, after application of a proposed methodology for fuzzy logic function synthesis, the circuit structure was substantially reduced.Figure 6 illustrates only the simulated graph of mem-

bership function I(RL), and the theoretical membership function MEMFUN(X).

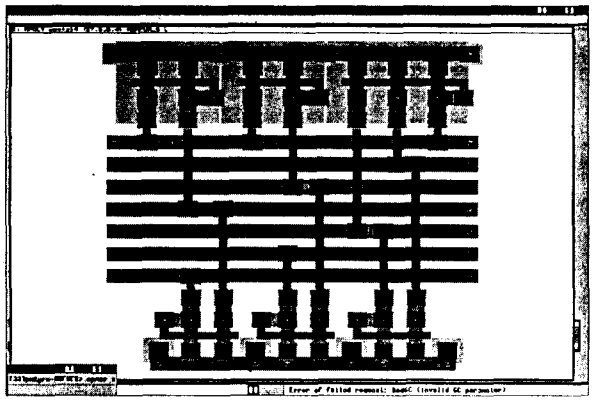

Figure 5 The final layout generated for the membership function (MF) unit using the proposed framework.

Simulation was done using the same transistor models as in the previous example. The simulation results show much better accuracy, comparing to the results from the previous example. The maximum error hardly reaches 15%. Due to the applied methodology of current mirror synthesis, the overall reduction in the number of transistors is expected to be up to 50%. As a result the total area occupied by the circuit is substantially reduced.

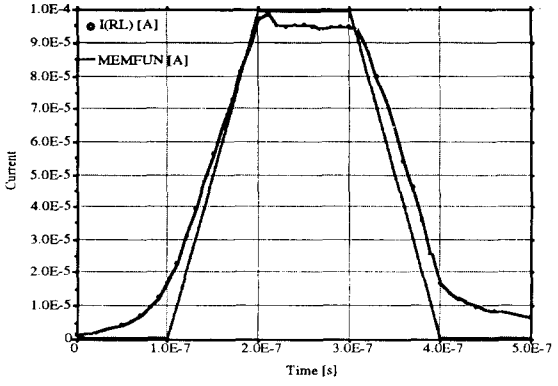

Figure 6 Results of HSPICE simulation I(RL) of the membership function unit (MF) generated using the proposed framework.

7. IMPLEMENTATION OF DOUBLE-INPUT SINGLE-OUTPUT FUZZY LOGIC CONTROLLER

To validate the proposed methodology and verify our prototype framework, 2-input-1-output fuzzy logic controller (FLC) was synthesized [6]. The circuit implementation of the FLC consists of only about 500 CMOS transistors. The premises and the output are described in terms of three linguistic values: Negative, Zero, and Positive, respectively. There are nine control rules embedded in this version of the controller. The netlist from FLC circuit was then extracted and simulated using HSPICE, and the final layout for the chip was generated (see Figure 7). The simulation results confirm the theoretical expectations regarding the complexity and performance of the resulting FLC circuit synthesized using the proposed approach. The test chip measurements shows that the typical circuit performance is 10MFLIPS, and the power consumption is 10mW.

8. CONCLUSIONS

The framework for automated synthesis of current-mode fuzzy logic circuits using the intelligent module is introduced. Current-mode CMOS fuzzy logic circuits are synthesized based on the new methodology also described in detail in [6]. The results of fuzzy logic controller circuit synthesis and simulation confirm the advantages of the proposed methodology over the classic methods of FL circuits design [5], [7], [9]-[11] in terms of the area and performance trade-offs. Up to 50% of the total area occupied by the circuit synthesized using our methodology can be saved. Also, the overall performance can be enhanced by up to 25%, over classically designed analog fuzzy logic circuits working in the current mode.

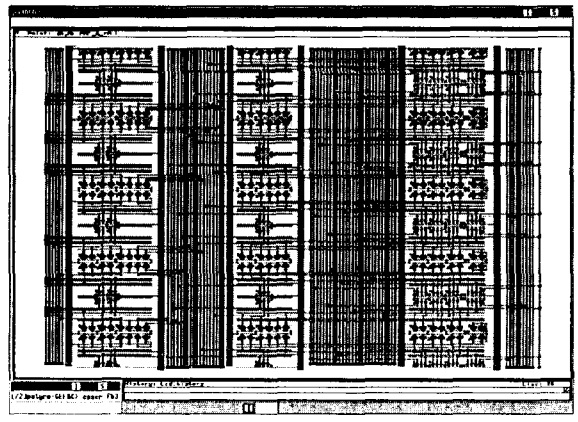

Figure 7 The final layout generated for the Double-Input Single-Output analog fuzzy logic controller.

9. REFERENCES

[1] R. Bowman, "Analog Integrated Circuit Design Conceptualization", in Introduction to Analog VLSI Design Automation, M. Ismail and J. Franca (editors), Kluwer Academic Publishers, pp. 1-27, Boston, 1990.

[2] J. Cohn et al., "KOAN/ANAGRAM II: New Tools for Device-Level Analog Placement and Routing", IEEE JSSC, vol. 26, no. 3, pp. 330-342, March 1991.

[3] GDT Designer Manuals, Mentor Graphics Corporation, San Jose, CA, November 1990.

[4] Hspice User's Manual, META-Software, Inc., Campbell, CA, 1991.

[5] L. T. Koczy, K. Hirota, "Digital Circuits Based on Algebraic Fuzzy Operations", Kluwer Academic Publ., pp. 101-114, 1990.

[6] L. Lemaitre, M. Patyra, and D. Mlynek, "Integrated CMOS Fuzzy Logic Functions: A Current Mirror Based Approach", IEEE CICC'93, San Diego, CA, May 1993.

[7] M. J. Patyra, "VLSI Implementation of Fuzzy-Logic Circuits", Fourth International Fuzzy Systems Association World Congress, Brussels, Belgium, June 1991.

[8] VEE-Test Reference Manuals *(Draft)*, Hewlett-Packard, April 1991.

[9] T. Yamakawa, T. Miki, "The current mode fuzzy logic integrated circuits fabricated by the standard CMOS process", IEEE Trans. Comp., (C-35), 161-167, 1986.

[10] L. Zhijian, J. Hong, A CMOS current-mode, high speed fuzzy logic microprocessor for a real-time expert system, Proc. of 20th Int'l. Symp. on MVL, Charlotte, USA, 1990.