

# PECVD BPSG Film 형성 및 Flow 특성

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Chemically vapor-deposited borophosphosilicate glass(BPSG) has become an essential insulating material for modifying the topography of advanced multilevel silicon-gate MOS intergrated circuits. Device contours have near-vertical steps and trenches that are formed by the patterned layers of insulators and high-temperature conductors. To ensure the continuity and integrity of subsequently deposited conductor layers the topography needs to be modified to produce a gradual taper over the edges and bottom corners of steps. This contour modification can be attained by thermal fusion flow of a CVD-BPSG layer under conditions that result in just enough viscous glass flow to form a tapered step profile. Device structures with relatively large feature size geometries of several microns have been processed successfully by this technique. Advanced ULSI circuits, however, require counters that approach planarity to allow the building of reliable multilevel structures. This paper represents a new BPSG planarization process using a multistage PECVD system made by Novellus.

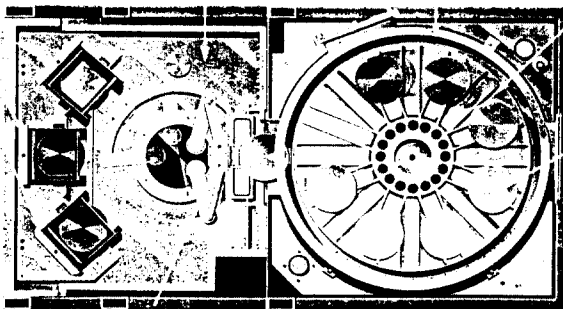
5000Å BPSG (4 wt % B, 4.7 wt % P)  
reflowed at 850°C in nitrogen (10  
minutes) and steam (10 minutes).



Cassettes hold  
up to 75 wafers.

Loadlock

Process chamber



Wafers are sequentially moved through 7 deposition stations, receiving a portion of deposition at each station.

Wafers are moved on a rotating spindle which recesses into the heater block during deposition.

Robot moves unfinished wafers into process chamber one at a time after removing finished wafers.