A New Approach to Advanced Poly-Silicon Deposition Technology

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As device dimensions continue to scale down, all processes are challenged by the issues of interface control, defects and contamination level, and more difficult three dimensional structures. Add to this the move to larger wafer diameters and most well charaterized processes must be retuned for manufacturability. A perfect example of this is in the deposition of polysilicon. For years the domain of large batch LPCVD horizontal tubes and more recently vertical tube furnaces, the demand for an even higher level of poly capability has begun to cause this dependable technology to be reexamined for adaptability to the demands of the 1990's

In particular, difficulty in doping *in-situ* with excellent uniformity of thickness and dopant, and control of the poly-to-silicon interface while maintaining acceptable throughput have begun to limit the future of conventional tube furnace technologies.

We report on charateristics of polysilicon deposited in a new concept single wafer system. The accelerated growth rates (in excess of 2000Å/min) allow practical implementation of single wafer performance in a production worthy environment. We demonstrate film characteristics that meet the needs of the most advanced integrated circuits. The enabling capability from our approach includes *in-situ* interface control, dopant control, and the ability to control crystalline structure.

Furthermore, we present a practical process by which integrated process technology can be realistically implemented.