Performance Analysis of the Knockout Switch with Input Buffer

서재준 (포항공과대학 산업공학과)
전치혁 (포항공과대학 산업공학과)

Since Asynchronous Transfer Mode (ATM) switching technology was recognized to be appropriate for broadband ISDN, various ATM switching architectures have been proposed. As is well known by one of them, the Knockout Switch is structured by single-stage and adopts output buffering method. The Knockout Switch seems to be excellent in traffic performancee (e.g., maximum throughput, delay and cell loss probability etc.), but it needs so many switch elements and buffers.

In this paper, the Knockout Switch with input buffer is proposed for the purpose of reducing the number of switch elements and buffers. We analyze the traffic performance and the complexity (i.e., the number of switch elements and buffers required) of the proposed architecture and compare with those of the existing Knockout Switch. It is found that the Knockout Switch with input buffer could reduce more than 40 % of switch elements and more than 30 % of buffers, respectively, without degrading the traffic performance.