CLAMP MODE에서 동작하는 ZVS-MRC FORWARD 콘버어터에 관한 연구

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THE CLAMP MODE FORWARD ZERO-VOLTAGE-SWITCHING MULTI-RESONANT-CONVERTER

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ABSTRACT

The clamp mode Zero-Volatge-Switched Multi-Resonant -Converter (ZVS-MRC) is proposed. In the converter, the performance of the conventional ZVS-MRC is improved by clamping the drain-to-source voltage of the power switch using a soft switching nondissipative active clamp network. The analysis for each stage of the converter operation modes is presented and is verified by experiments.

I. INTRODUCTION

The SMPS (Switch Mode Power Supply) by PWM (Pulse Width Modulation) has been successfully used for many years. However, there are some disadvantages for operating in high switching frequency, that is, parasitic reactance of the power circuit causes switching stress, power loss and noise. And the stored energy in the wiring and the transformer leakage inductance cause parasitic oscillation and voltage stress exists across drain-source of the power MOSFET (as a main switch) at turn off time.

The ZVS-QRCs have the capability of operating at high frequency, but also have two major limitation. One of the problems is excessive voltage stress at the switching transistor. This voltage stress is proportional to the load range, which make it difficult to implement ZVS-QRCs in applications where the load varies over a wide range. Other problem is caused by the parasitic junction capacitance of the rectifying diode. There are some parasitic oscillations of the resonant inductance and rectifier's capacitance occur in the circuit. If damped, these oscillation cause power dissipation. If undamped, they adversely effect the voltage gain of the converter, which makes the converter difficult to control [6].

ZVS-MRC can absorb all the major parasitic components, including transistor output capacitance, diode junction capacitance, and transformer leakage inductance into the resonant cicuit. With these characteristics, ZVS-MRCs have the capability of handling a very wide load range with much reduced voltage stress compared to their QRC counterparts. However, the voltage stress across the MOSFET switch of the ZVS-MRCs is still high as it is compared to that of the PWM type converters. Typically, the voltage stress in ZVS-MRCs is four times the supply voltage. This limits the use of ZVS-MRCs in off-time applications. Furthermore, conduction loss of MOSFET is also increased due to the use of higer voltage rating devices.

This paper proposes a method of improving ZVS-MRC by employing a soft switching nondissipative active clamp network. Clamping action is obtaind by placing, in parallel with the power switch, a series combination of active switch and clamping capacitor, so that the voltage stress across the main switch is clamped to minimum value.

This paper presents the analysis for each stage of the converter operation modes and the experimental result on the converter.

II. FORWARD ZVS MRC

1.FORWARD ZVS-MRC

The basic circuit of forward ZVS-MRC is shown in Fig.1, which operates with wide load range and automatic reseting of the transformer. The forward ZVS MRC is isolated between the primary and the secondary sides of transformer. There are three resonant components at the power circuit: a primary resonant inductor L_R, a primary resonant capacitor C_R in parallel with the main switch and a secondary resonant capacitor C_D. These resonant elements absorb the parasitic reactance of active, passive switches and leakage inductance of transformer. The junction capacitance C_{oss} of power MOSFET is absorbed in C_R, the junction capacitance of rectifying diode is absorbed in C_D, and the leakage inductance of transformer is absorbed in L_R in series.

Because the peak voltage stress at turn off time is one of the problems in forward ZVS MRC, we must find the best way and new technique to reduce this voltage stress.

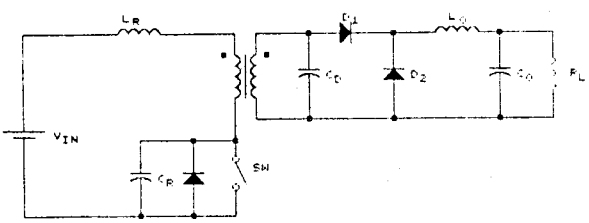


Fig.1 The basic circuit of Forward ZVS-MRC

2. THE CLAMP MODE FORWARD ZVS-MRC

Fig.2 shows the CMF ZVS-MRC (Clamp Mode Forward Zero Voltage Switching Multi Resonant Converter), it also implements zero voltage switching and utilizes all parasitic reactance of the power circuit.

The converter is derived from the forward ZVS-MRC topologies by adding the clamp circuit to the primary side of power circuit. The clamp circuit components are: a clamp capacitor C_C placed at primary side, and the switch SW_2 in series with the clamp capacitor, the clamp circuit is parallel with the primary resonant capacitor C_R and the main switch SW_1. The capacitor C_C and SW_2 is activated for clamping peak voltage stress of the main switch SW_1 at turn off time.

This proposed converter also has the capability such as the conventional ZVS-MRC. The leakage inductance of the transformer is absorbed into resonant inductor, the junction capacitance of SW_2 into clamp capacitor C_C, and the junction capacitance of SW_1 into the resonant capacitor C_R. Also, C_D provides automatic resetting of transformer.

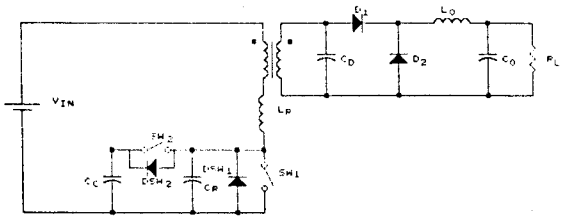


Fig.2 The Clamp Mode Forward ZVS MRC

III. ANALYSIS OF THE CIRCUIT OPERATION

Fig.3 shows an eqivalent circuit of the clamp mode forward ZVS-MRC.

The following assumptions are used in the analysis:

a) the output filter inductance is sufficiently large to be approximated by a current source with a value equal to the output current Io;
b) the transfomer turns ratio of the primary to the secondary side is unity (N=1);
c) the magnetizing inductance of the power transfomer is large and can be represented by an equivalent current source, Im, whose magnitude depends on the operating condition but is constant over one switching cycle;
d) The voltage drop across the conducting semiconductor switches (MOSFETs and diodes) is negligible, and all fundamental elements of circuit is ideal; and
e) the active and the passive switch element at the semiconductor device are ideal, i.e each switching elements implement zero voltage switching.

To simplify the analysis further, the load current, Io, and the resonant capacitor C_D, are reflected to the primary side of the transformer and the rectifying diodes are replaced by a SPDT switch. When the voltage across C_D, V_d, is positive, the forward diode D_1 is ON and D_2 is OFF, the switch is at position 1. When it is negative, diode D_1 is OFF and D_2 is ON, it is at position 2.

The topological stage of circuit diagrams during one cycle switcing are shown in Fig.4, where the converter can operate in six different modes. Each mode represents a different sequence of topological stages. The sequence at the topological stages is A-B-C-D-E-F. Fig.4(b) shows the waveforms of the clamp mode forward ZVS-MRC in various mode of operation.

The expressions of the resonant current for each topological stages are as follows:

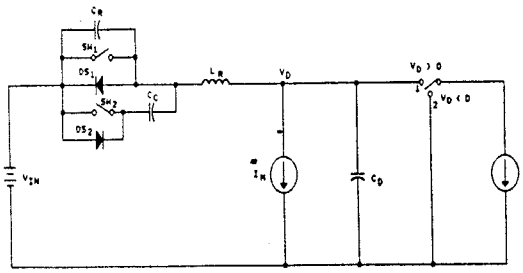


Fig.3 The eqivalent circuit diagram

$$I_e = \begin{cases} I_m & \text{for A} \\ I_m + I_o & \text{for A,B,C,D,E} \end{cases}$$

for stages A and B

$$\omega_n = \frac{1}{\sqrt{L_R C_D}} \qquad Z_n = \sqrt{\frac{L_R}{C_D}}$$

for stages C and F

$$C_o = \frac{C_D C_R}{C_R + C_D} \quad , \quad \omega_o = \frac{1}{\sqrt{L_R C_o}} \quad , \quad Z_o = \sqrt{\frac{L_R}{C_o}}$$

and for stages D and E

$$C_s = \frac{C_D C_C}{C_C + C_D} \quad , \quad \omega_s = \frac{1}{\sqrt{L_R C_s}} \quad , \quad Z_s = \sqrt{\frac{L_R}{C_s}}$$

Stage A [$t_o \sim t_1$]

During this stage switch SW_1 and D_2 are conducting (on), and SW_2 and D_1 is off and voltage $V_D(t)$ across capacitor C_D is negative. Resonant inductor L_R and capacitor C_D cause $i_{LR}(t)$ to increase. This stage ends at $t=t_1$ when voltage V_D increase to zero, diode D_1 turn on and D_2 to turn off. From Fig.4(a) we obtain $i_{LR}(t)$ and $V_D(t)$ as follows:

$$i_{LR}(t) = \frac{V_{IN}}{Z_n} \sin\omega_n t + i_{LR}(t_o)\cos\omega_n t \qquad (1)$$

$$V_D(t) = V_{IN}[1-\cos\omega_n t] + i_{LR}(t_o)\, Z_n \sin\omega_n t + V_D(t_o) \qquad (2)$$

Stage B [$t_1 \sim ta_2$]

$V_D(t)$ increase from zero to the positive value, and the resonant current $i_{LR}(t)$ reach the peak value. At the end of this stage, the SW_1 turn OFF.

$$i_{LR}(t) = \frac{V_{IN}}{Z_n} \sin\omega_n t + [i_{LR}(t_1) - I_e]\cos\omega_n t + I_e \qquad (3)$$

$$V_D(t) = V_{IN}[1-\cos\omega_n t] + [i_{LR}(t_1) - I_e]\cos\omega_n t + V_D(t_1) \qquad (4)$$

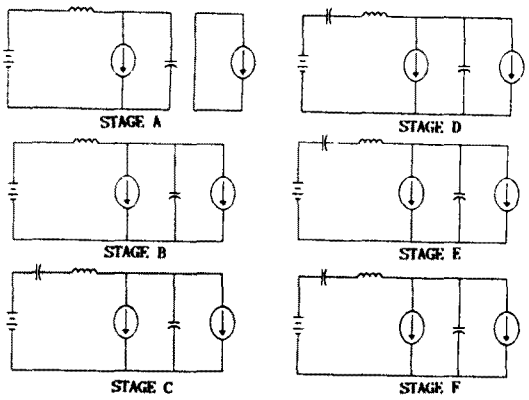
Stage C [$t_2 \sim t_3$]

After the main switch SW_1 is turn off, $i_{LR}(t)$ and $V_C(t)$ are resonated by the three resonant elements L_R, C_R and C_D. V_{DS1} are inceased during this stage. $i_{LR}(t)$, $V_D(t)$ and the voltage across the drain and source of switch SW_1, $V_{DS1}(t)$ are obtained as follows: the

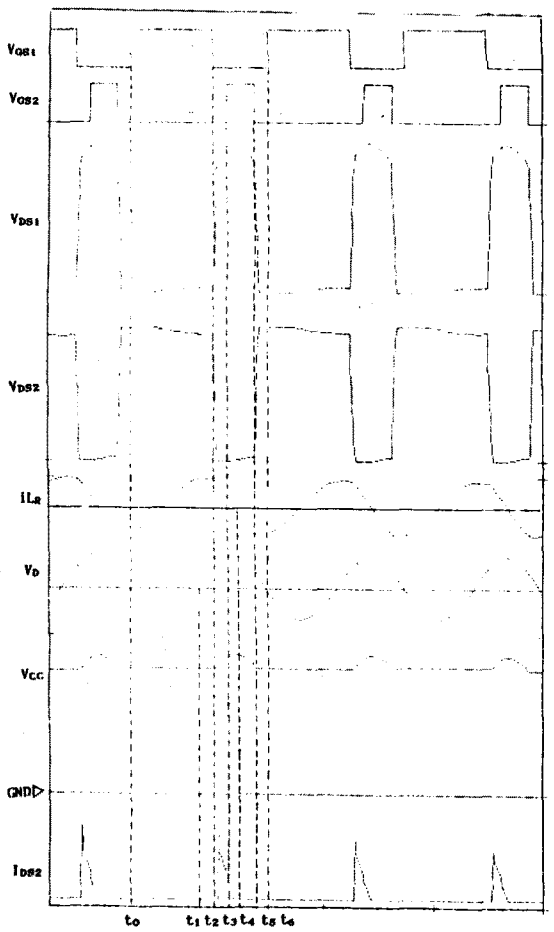
$$i_{LR}(t) = \frac{V_{IN}}{Z_o} \sin\omega_o t + \left[i_{LR}(t_2) - \frac{I_e C_o}{C_D} \right] \cos\omega_o t + \frac{I_e C_o}{C_D} \qquad (5)$$

$$V_D(t) = \frac{V_{IN} C_o}{C_D}(1 - \cos\omega_o t) + \left[\frac{i_{LR}(t_2)}{C_D \omega_o} - \frac{I_e C_o}{\omega_o C_D^2} \right] \sin\omega_o t + V_D(t_2) + \left[\frac{I_e C_o}{C_D^2} - \frac{I_e}{C_D} \right] t \qquad (6)$$

$$V_{DS1}(t)=\frac{V_{IN}C_o}{C_R}(1-\cos\omega_o t)+\left\{\frac{i_{LR}(t_2)}{C_R\omega_o}-\frac{I_eC_o}{C_DC_R\omega_o}\right\}\sin\omega_o t + \frac{I_oC_o}{C_DC_R}t \quad (7)$$



(a)The topological stages of CM Forward ZVS MRC



(b) Theoretical waveforms

Fig. 4 The topological stage and theoretical waveforms for each mode of CM Forward ZVS MRC

Stage D [$t_3 \sim t_4$]

In this stage, switch SW_2 is turn on, and the valtage across the capacitor, C_C, is more and more increased. As a result, voltage $V_{DS1}(t)$ is clamped by the voltage across the cpacitor, C_C, and $i_{LR}(t)$ decrease to zero.

$$i_{LR}(t)=\frac{V_{IN}}{Z_S}\sin\omega_s t+\left\{i_{LR}(t_3)-\frac{I_eC_S}{C_D}\right\}\cos\omega_s t+\frac{I_eC_S}{C_D} \quad (8)$$

$$V_D(t)=\frac{V_{IN}C_S}{C_D}(1-\cos\omega_s t)+\left\{\frac{i_{LR}(t_3)}{C_D\omega_s}-\frac{I_eC_S}{\omega_sC_D^2}\right\}\sin\omega_s t + V_D(t_3)+\left\{\frac{I_eC_S}{C_D^2}-\frac{I_e}{C_D}\right\}t \quad (8)$$

$$V_{DS1}(t)=\frac{V_{IN}C_S}{C_C}(1-\cos\omega_s t)+\left\{\frac{i_{LR}(t_3)}{C_C\omega_s}-\frac{I_eC_S}{\omega_sC_DC_C}\right\}\sin\omega_s t + \frac{I_oC_S}{C_DC_C}t + V_{DS1}(t_3) \quad (10)$$

Stage E [$t_4 \sim t_5$]

Switch SW_2 remains on, the voltage across the capacitor, C_C, will decrease to the constant value, and the voltage, $V_{DS1}(t)$, is still clamped. This stage ends at $t=t_5$, when switch SW_2 is turned off.

$$i_{LR}(t)=\frac{V_{IN}}{Z_S}\sin\omega_s t+\left\{i_{LR}(t_4)-\frac{I_eC_S}{C_D}\right\}\cos\omega_s t+\frac{I_eC_S}{C_D} \quad (11)$$

$$V_D(t)=\frac{V_{IN}C_S}{C_D}(1-\cos\omega_s t)+\left\{\frac{i_{LR}(t_4)}{\omega_sC_D}-\frac{I_eC_S}{\omega_sC_DC_C}\right\}\sin\omega_s t + V_D(t_4)+\left\{\frac{I_oC_S}{C_D^2}-\frac{I_e}{C_D}\right\}t \quad (12)$$

$$V_{DS1}(t)=\frac{V_{IN}C_S}{C_C}(1-\cos\omega_s t)+\left\{\frac{i_{LR}(t_4)}{C_C\omega_s}-\frac{I_eC_S}{C_DC_C\omega_s}\right\}\sin\omega_s t + V_{DS1}(t_4) \quad (13)$$

Stage F [$t_5 \sim t_6$]

Main switch SW_1 and clamp switch SW_2 are turn off, the voltage across the S_{W1} $V_{DS1}(t)$ and $V_D(t)$ is reduced to zero. The cycle is completed when the switch SW_1 is turned on at $t=t_6$.

$$i_{LR}(t)=\frac{V_{IN}}{Z_o}\sin\omega_o t+\left\{i_{LR}(t_5)-\frac{I_eC_o}{C_D}\right\}\cos\omega_o t+\frac{I_eC_o}{C_D} \quad (14)$$

$$V_D(t)=\frac{V_{IN}C_o}{C_D}(1-\cos\omega_o t)+\left\{\frac{i_{LR}(t_5)}{C_D\omega_o}-\frac{I_eC_o}{C_D^2\omega_o}\right\}\sin\omega_o t + \left\{\frac{I_eC_o}{C_D^2}-\frac{I_e}{C_D}\right\}t + V_D(t_5) \quad (15)$$

$$V_{DS1}(t)=\frac{V_{IN}C_o}{C_R}(1-\cos\omega_o t)+\left\{\frac{i_{LR}(t_5)}{C_R\omega_o}-\frac{I_eC_o}{C_DC_R\omega_o}\right\}\sin\omega_o t + \frac{I_eC_o}{C_DC_R}t+\frac{V_{DS1}(t_5)}{C_R} \quad (16)$$

IV. EXPERIMENT RESULT

A clamp mode Farward ZVS-MRC was breadborded with the following specification.

- o Output Voltage V_o = 5 [V]
- o Input Voltage V_{IN} = 48 [V] ±10 [V]
- o Maximum switching frequency $f_{s\ max}$ = above 2 [MHz]
- o Maximum output current = 7 [A]

Fig.5 shows the clamp mode forward ZVS MRC with circuit diagram of the converter including gate drive, VCO (Voltage Control Oscillator) and error amplifier using in experiment.

Fig.6 shows oscillograms for the clamp mode Froward ZVS-MRC. Fig.7 shows switching voltage stress of Vds1 versus switching frequency, Fig.8 shows the voltage stress of Vds1 versus the Duty (f_{2ON}/f_{1OFF}) variation. Fig.9 shows the stability of output voltage versus load variation measured from the experimental power stage.

V. CONCLUSIONS

The analysis and experiments of the clamp mode forward ZVS-MRC are carried out under the conditions of 5V/7A output and 2MHz switching frequency. As a result, we obtain the followings:

1) Voltage stress across the main switch is 150V at full load.
2) 80% efficiency and less than 1% regulation error at full load.
3) Zero-Voltage-Switching is also achived in the clamping circuit.

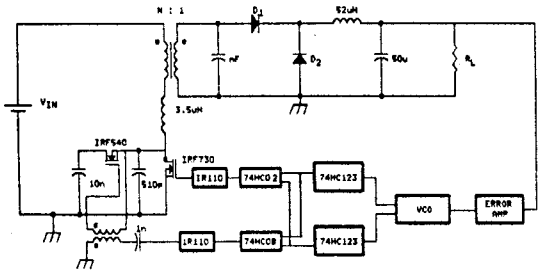
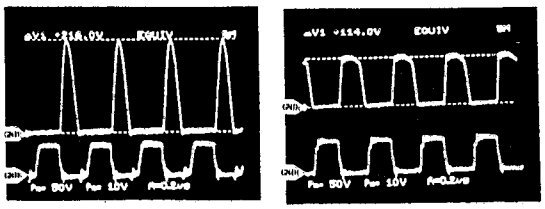
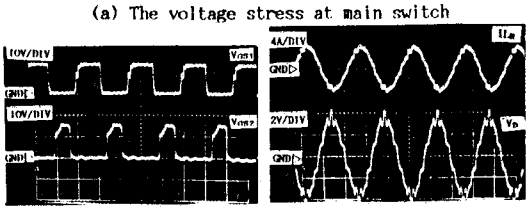


Fig.5 The clamp mode Forward ZVS-MRC with control circuit

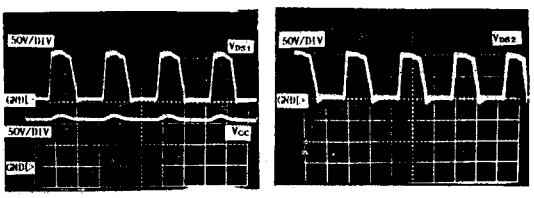


Conventional ZVS-MRC CMF ZVS-MRC

(a) The voltage stress at main switch



(b) Gate signal of SW_1 and SW_2 (c) i_{LR} and V_D



(d) V_{DS1} and Vcc (e) V_{DS2}

Fig.6 The oscillograms for the CM Forward ZVS-MRC.

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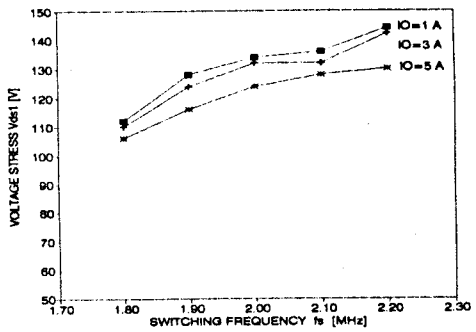

Fig.7.The voltage stress of V_{ds1} versus switching frequency

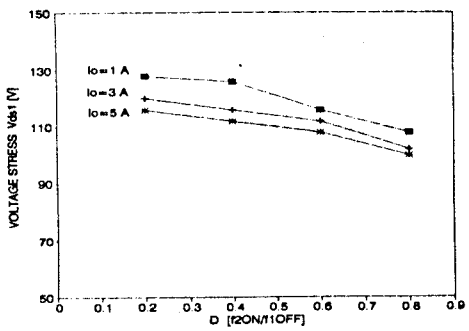

Fig.8 The voltage stress V_{ds1} versus the Duty variation.

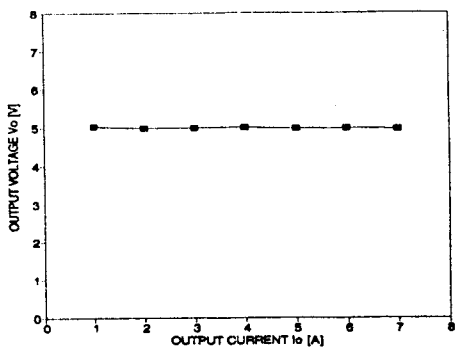

Fig.9 The stability of output voltage versus load variation