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Analysis of Differential Non-linearity of Successive Approxination ADC

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Abstract: The channel irregularity of Successive Approximation ADC is very large in comparison with other type of ADCs. This characteristic makes it impossible to apply the Successive Approximation ADC to the field of radiation pulse height analysis or the measurement of probability density function. In this paper,an analysis of differential non-linearity of this ADC is presented. It is made clear that the small deviation of resistance causes very large differential non-linearity.

1. Introduction

The successive approximation ADC (SAADC) is a very popular ADC and has very short conversion time but has large differential non-linearity (DNL). Because of this reason, SAADC is seldom used for the pulse height analysis (PHA) on radiation measurement.[1)]

The Wilkinson type ADC is still extensively used for the PHA, but it has very long conversion time.[1)2)] The most famous rearch to apply the SAADC to PHA eliminating the DNL is Gatti's "Sliding Scale Method" reported. 28 years befor approximately.[1)3)4)] The DNL error is the most difficult error to deal with since it cannot be eliminated by adjustment.

The largest cause for the DNL of SAADC is due to the deviation in the output analog difference of included D/A converter (DAC) between two adjacent code from the ideal value. In this paper, at first, the DNL of SAADC is analyzed using admittance matrix of ladder-type resistance network. After the analysis and the computer simulation, the following properties become evident.

(1) The resistance errors cause DNL at the specially fixed 2 channels.
(2) The small resistance error cause considerably large DNL.
(3) It becomes possible to calculate the correction factor making use of the results of this analysis.

2. DNL analysis for SAADC

The SAADC includes DAC in it and compare input analog signal to output analog signal of the DAC. Because of this procedure, the deviation in the output analog difference of included DAC between two adjacent code from the ideal value appears directly to the DNL of the SAADC. The Ladder-type resistance network is a typical example of DAC. The output analog difference of this DAC is analyzed as the DNL of SAADC.

Block diagram of SAADC is shown in Fig.1.

The resistances which constitute the ladder-type resistance network are given by

$$R_{1k} = R+\Delta R_{1k},(k=1,2,\ldots,n-1) \quad (1)$$
$$R_{2k} = 2R+\Delta R_{2k},(k=1,2,\ldots,n) \quad (2)$$
$$G_{1k} = 1/R_{1k},(k=1,2,\ldots,n-1) \quad (3)$$
$$G_{2k} = 1/R_{2k},(k=1,2,\ldots,n) \quad (4)$$

Where, ΔR_{1k} and ΔR_{2k} are the resistance errors respectively. G_{1k} and G_{2k} are the conductances. Let G_M and G_L be parallel conductances to G_{21},G_{2n} respectively.

Let $v_1,v_2,\ldots,v_n$ be the node voltages.

Let $i_1,i_2,\ldots,i_n$ be the currents flow into every nodes. n is the bit number.

The relation between i_k and v_k (k=1,2, ...,n) is presented as equation (5).

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ \\ \\ i_n \end{bmatrix} = \begin{bmatrix} (G_M+G_{21}+G_{11}) & -G_{11} & & & & \\ -G_{11} & (G_{11}+G_{22}+G_{12}) & -G_{12} & & 0 & \\ & -G_{12} & (G_{12}+G_{23}+G_{13}) & -G_{13} & & \\ & & & & -G_{1,n-2} & \\ & 0 & & & (G_{1,n-1}+G_{2,n-1}+G_{1,n-1}) & -G_{1,n-1} \\ & & & & -G_{1,n-1} & (G_{1,n-1}+G_{2n}+G_L) \end{bmatrix} \times \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ \\ \\ v_n \end{bmatrix} \quad (5)$$

From eqn.(5), it follows that

$$[V] = \left[I_1/G_{21}, I_2/G_{22}, \ldots, I_n/G_{2n}\right]^T$$

$$= [G]^{-1}[I] = \frac{1}{\det[G]} \cdot \left[\mathrm{adj}[G]\right]^T \cdot [I] \quad (6)$$

Where, $I_1, I_2, \ldots, I_n$ are the 2^n weighted currents flowing through $R_{21}, R_{22}, \ldots, R_{2n}$ respectively. And $[I] = [I_0, 0, 0, \ldots, 0]^T$ (7)

I_0 : constant current

$\det[G] \neq 0$

From eqn.(6),

$$v_k = \frac{I_k}{G_{2k}} = \frac{[\mathrm{adj}[G]]_{1k}}{\det G} \cdot I_0, (k=1,2,\ldots,n) \quad (8)$$

$$I_k = \frac{G_{2k} \cdot \Delta_{1k} \cdot I_0}{\det[G]}, (k=1,2,\ldots,n) \quad (9)$$

Where, Δ_{1k} is adjoint matrix of G_{1k}

The DAC output current is given as

$$I_{out} = I_1S_1 + I_2S_2 + \ldots + I_nS_n = \sum_{i=1}^{n} I_iS_i \quad (10)$$

Where, $S_1, S_2, \ldots, S_n$ are the input code consist of 0 or 1. (S_1:MSB, S_n:LSB)

Combining eqns.(9) with (10) yields

$$I_{out} = \sum_{k=1}^{n} \frac{G_{2k} \cdot \Delta_{1k} \cdot I_0}{\det[G]} \cdot S_k \quad (11)$$

Let I^B_{out} be the DAC output current in the case of that the input code is binary B($0 \sim 2^{n-1}$). And let k-th bit of B be S^B_k.

The output analog current difference of DAC between two adjacent binary code B and B+1 is expressed as

$$\Delta I^B_{out} = I^{B+1}_{out} - I^B_{out}$$

$$= \frac{I_0}{\det[G]} \left(\sum_{k-1}^{n} G_{2k} \cdot \Delta_{1k} \cdot S^{B+1}_k - \sum_{k-1}^{n} G_{2k} \cdot \Delta_{1k} \cdot S^B_k \right) \quad (12)$$

Where, $B = 0 \sim 2^n - 2$

The DNL is defined from eqn.(12) as follow

$$DNL = \frac{\left[\Delta I^B_{out} - \left[\Delta I^B_{out}\right]_{ave}\right]_{max}}{\left[\Delta I^B_{out}\right]_{ave}} 100[\%] \quad (13)$$

Where,

$$\left[\Delta I^B_{out}\right]_{ave} = \frac{1}{2^n - 1} \sum_{B=0}^{2^n-2} \Delta I^B_{out} \quad (14)$$

$[\cdot]_{max}$: maximum, $[\cdot]_{ave}$: average

3. Example of computation

In this section, the object is to show a simple example of computation in the case of n = 4.

The admittance matrix is as follow

$$[G] = \begin{bmatrix} (G_M+G_{21}+G_{11}) & -G_{11} & & \\ -G_{11} & (G_{11}+G_{22}+G_{12}) & -G12 & 0 \\ & -G_{12} & (G_{12}+G_{23}+G_{13}) & -G_{13} \\ 0 & & -G_{13} & (G_{13}+G_{24}+G_L) \end{bmatrix} \quad (15)$$

The DNL having e[%] error of R_{22} is computed as follow.

$$DNL = \frac{\Delta I^3_{out} - I_T/15}{I_T/15} \times 100\ [\%]$$

$$= \frac{-54e}{1500 + 9e} \times 100\ [\%] \quad (16)$$

Where,

$$e = \frac{\Delta R_{22}}{2R} \times 100\ [\%] \quad (17)$$

$$\Delta I^3_{out} = I^4_{out} - I^3_{out} \quad (18)$$

$$= \frac{I_0}{\det[G]} \left(G_{22} \cdot \Delta_{12} - G_{23} \cdot \Delta_{13} - G_{24} \cdot \Delta_{14} \right) \quad (19)$$

$$I_T = I_1 + I_2 + I_3 + I_4 = \frac{I_0}{\det[G]} \sum_{k=1}^{4} \left(G_{2k} \cdot \Delta_{1k} \right) \quad (20)$$

From eqn.(16), the relations between e and the DNL are shown in Table 1.

Table 1

e [%]	DNL [%]
0.00	0.00
0.05	0.14
0.10	0.32
0.20	0.68
0.50	1.76
1.00	3.54
5.00	17.48

Fig.2 shows the DNL corresponding to the channel width of SAADC in case of every resistances are gived small error independently.

4. Conclusion

The channel width error of SAADC is analyzed in this paper. The followings are clarified.

(1) From Fig.2, the channel width of SAADC has distinctive feature at the 2^n-th channels.

(2) From Table 1, Fig.3(a) and(b), small resistance error cause large DNL error.

(3) It becomes able to find out the correction factor using the results of this analysis. Because, the DNL error is treated as a systematic error, not as a accidental error.

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References

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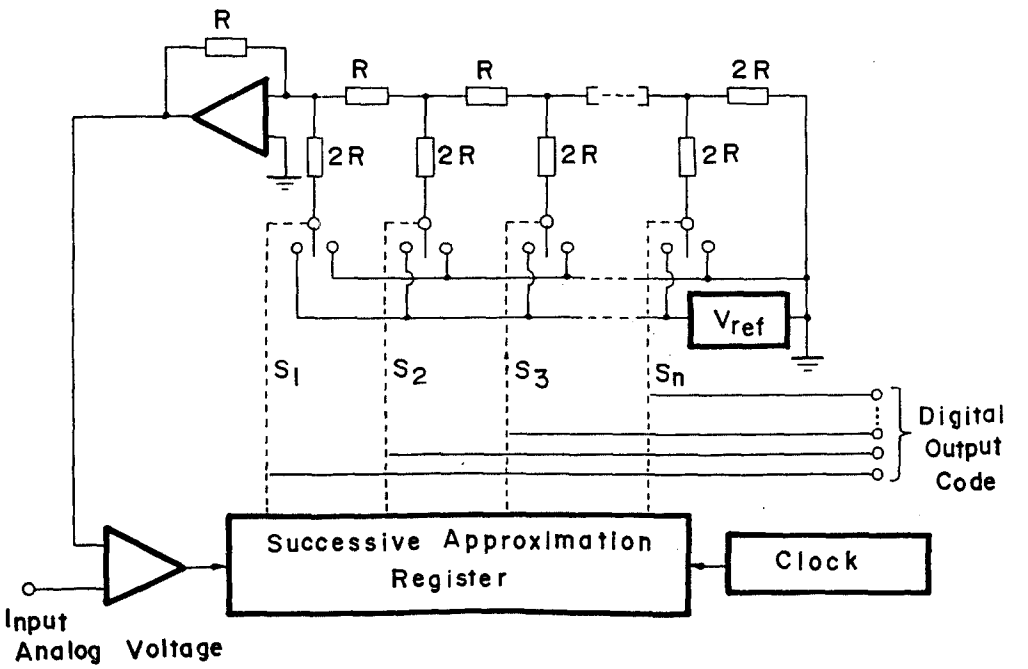

Fig.1 Block diagram of successive approximation ADC (SAADC)

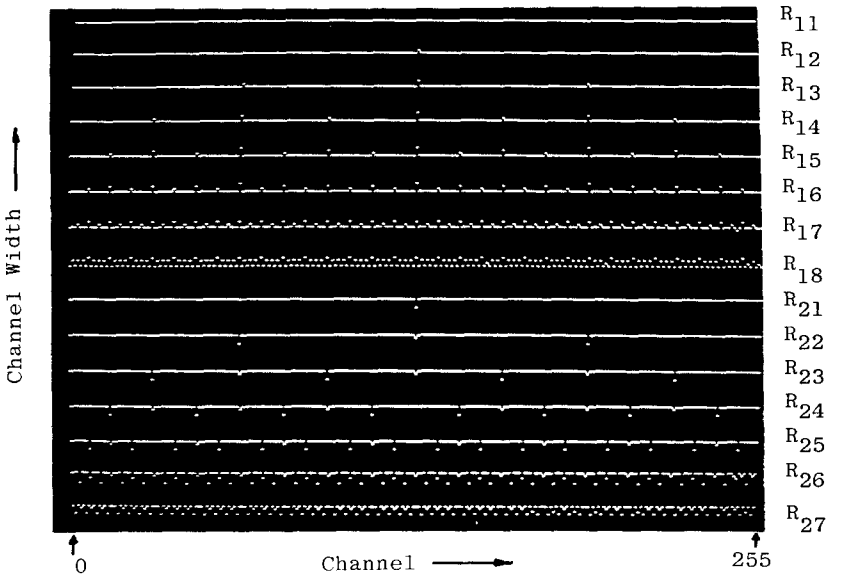

Fig.2 Channel width of SAADC caused by each independent resistance error

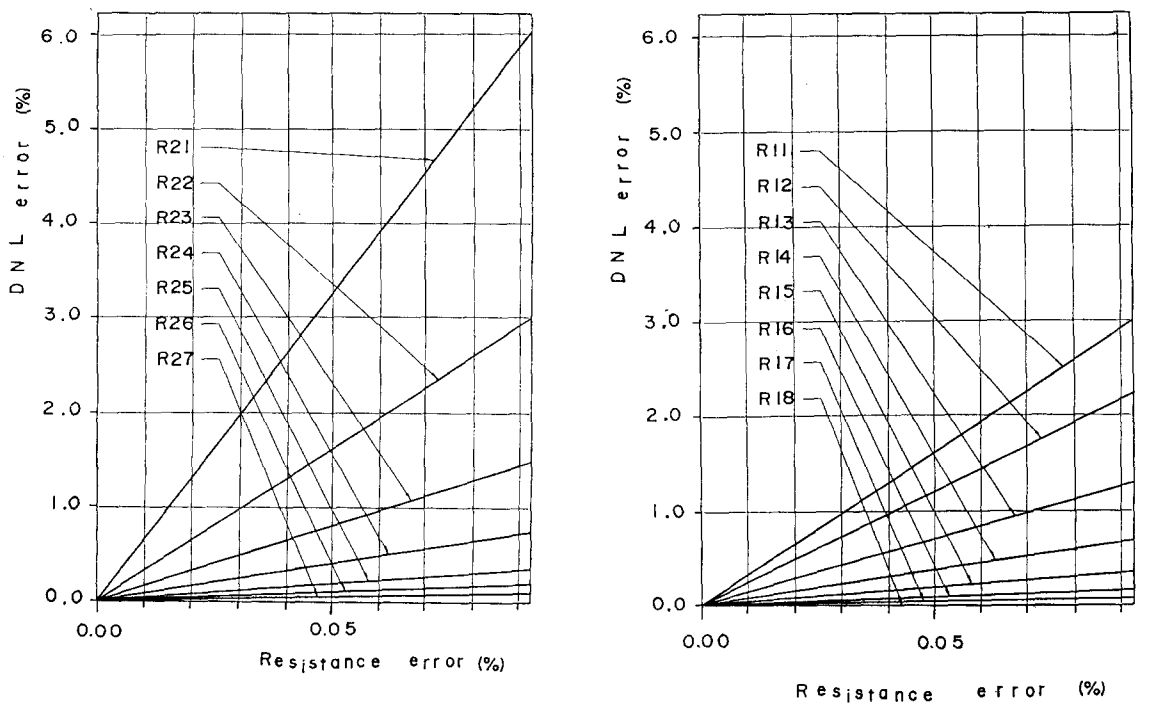

Fig.3 Computed DNL error of SAADC for each independent resistance error