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Wave Digital Filter의 설계 및 특성에 관한 연구

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On the Design and Properties of Wave Digital Filter

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Abstract

There has been a great amount of interest in the design of digital filters with low sensitivity to coefficient variations. Especially the wave digital filter modeled after analog LC ladder filter has been studied to have low-coefficient-sensitivity properties.

This paper examined the design of the wave digital filter and how the sensitivity and roundoff noise property arises. As a result of computer simulation the implementation of the digital filter was possible with a lower coefficient word length comparing with the conventional cascade structure.

1. Introduction

Digital filters are realized either with special-purpose digital hardware or as a computer algorithm. In both cases filter coefficients can only be expressed using a finite number of bits.

Furthermore, in many instances it may be advantageous to use as few bits as possible to express filter coefficients. But the small number of bits may lead to a system which does not satisfy any more the original filter characteristic and even result in an unstable system if the pole locations are near the unit circle in the Z-plane.

Therefore there has been a great amount of interest in the design of digital filters with low sensitivity with respect to coefficient variations.

Wave digital filter proposed by Fettweis which is modeled via transmission-line transformations from analog LC ladder networks has been showned to have the characteristic of low-coefficient-sensitivity.

This paper examines the design and properties of the wave digital filter. And then coefficient sensitivity properties are compared with the cascade form digital filter.

2. The Design of Wave Digital Filter

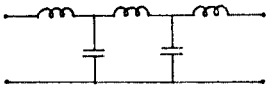

Fig.1 LC Ladder network

We examine the design of the wave digital filter where the frequency response of the digital filter will be a bilinear transformation of the frequency response of the analog filter such as a LC ladder network of Fig. 1.

(1) Richards' Transformation

The first step in the procedure is to perform a

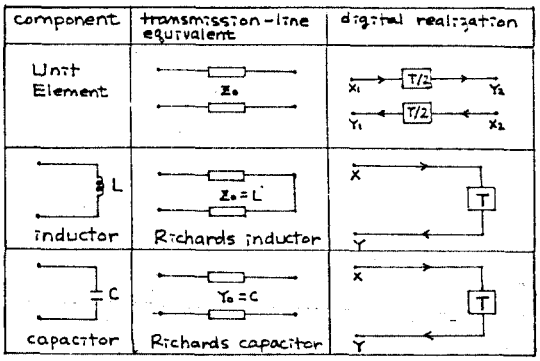

Fig.2. Unit Element and Richards elements

Richards transformation on the LC ladder network. This consists of replacing inductors with short-circuited delay lines and capacitors with open-circuilted delay lines. All of the delay lines are chosen to have equal delay T/2 and are referred to as unit elements.

The characteristic impedance Zo of Richards inductor are chosen to be equal to the inductance value and the characteristic admittance Yo of Richards capacitor are chosen to be equal to the capacitance value.

These tabled as follows.

	inductor	Richards inductor	capacitor	Richards capacitor
Complex impedance	sL	SZ_o	$\frac{1}{sC}$	$\frac{1}{SY_o}$

where

$$S = \tanh(sT/2) \qquad (1)$$

By the Richards transformation the frequency response of the filter become a bilinear transformation of the original response and all of the elements of the original filter is transformed into delay lines.

Since the delay lines are used as one-port elements the basic unit of delay in the operation of filter is the round-trip delay T. This delay is therefore consistent with the sampling period and it is conceivable that since the signals in the filter can be represented as sequences and the operation of the filter is based on unit T delays, the entire operation of the filter could be performed digitally.

In fact it is convenient to choose as the signal variables in the filter the forward-and reverse--raveling voltage waves. The digital filter in this case is then a digital implementation of the wave flow diagram of the analog filter.

(2) Series Line Interconnection

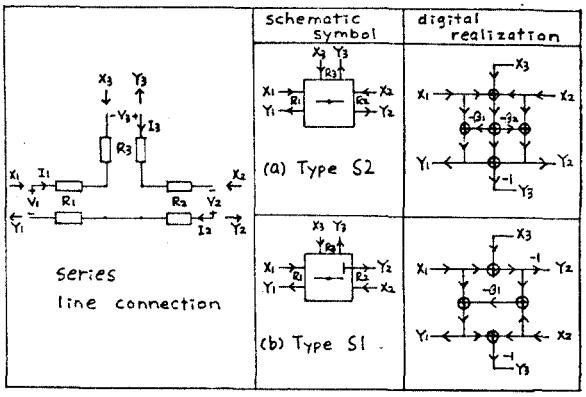

Fig.3 Three port series adaptors

The function of the three port series adaptor is to connect three ports in series whose characteristic impedances are R1, R2, and R3, respectively, as in Fig.3. The three port voltages and currents are related as follows:

$$I_1 = I_2 = I_3, \quad V1 + V2 + V3 = 0 \qquad (2)$$

The wave variables, X_K and Y_K, can be expressed in terms of the currents and voltages as follows:

$$X_K = V_K + I_K R_K, \quad Y_K = V_K - I_K R_K \qquad (3)$$

$$(k = 1, 2, 3)$$

Using (2) and (3),

$$\begin{bmatrix} Y_1 \\ Y_2 \\ Y_3 \end{bmatrix} = \begin{bmatrix} 1-\beta_1 & -\beta_1 & -\beta_1 \\ -\beta_2 & 1-\beta_2 & -\beta_2 \\ -\beta_3 & -\beta_3 & 1-\beta_3 \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \\ X_3 \end{bmatrix} \qquad (4a)$$

From (4b) $B_1 + B_2 + B_3 = 2$, therefore only two coefficients are necessary for implementing this set of equations and a structure for doing this is the series 2-multiplier adaptor (Type S2) of Fig. 3(a).

With R_2 unspecified, one can choose $R_2 = R_1 + R_3$ so that $B_1 = R_1/R_2$, $B_2 = 1$ according to Eq. (4b). As a consequence, the above adaptor can be simplified to the series 1-multiplier adaptor (Type S1) of Fig.3(b).

(3) Parallel Line Interconnection

A similar implementation can be established for the parallel connection.

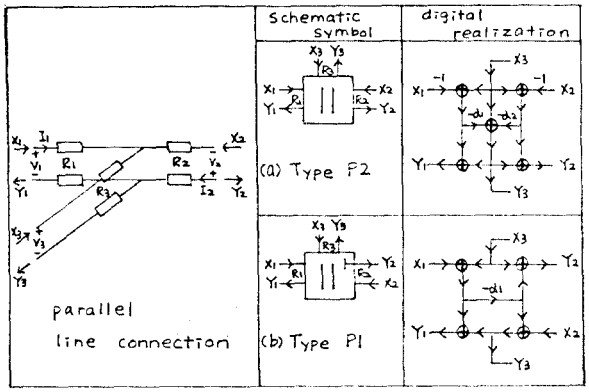

Fig.4. Three port parallel adaptors

(4) Digital Filter Realization

If a digital structure is constructed from an analog LC ladder design such as that of Fig. 1 it is necessary to directly interconnect three port series and three port parallel adaptors.

In this case digital networks containing delay-free loops are said to be unrealizable because certain node signals in such networks cannot be computed. Therefore, an important design rule is that every feedback loop must contain at least one delay.

A. Indirect Realization

If adaptor ports with direct paths are interconnected digital networks with inner loops without delay can arise. This problem can be solved by changing the topology of the unit element analog network to a form which has delays separating each junction. This is accomplished with the aid of Kuroda's identities.

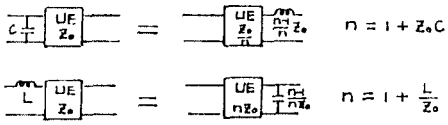

Fig.5 Kuroda's identities

B. Direct Realization

If adaptor ports with direct path are not interconnected digital networks can contain at least one delay.

The only adaptor port without direct paths is port 2 in adaptors S_1 and P_1, as in Figs 3 and 4. Therefore, for the sake of digital filter realization every direct connection between adaptor ports must necessarily involve port 2 of either an S_1 and a P_1 adaptor.

C. Mixed Realization

Digital filters can be realized in a way that certain substructures inside them are realized as direct realization, while others include indirect realization. Hence a large variety of mixed structure are available.

3. The Properties of Wave Digital Filter

(1) Attenuation Sensitivity

In the design of the wave digital filter an equally terminated LC ladder filter satisfying prescribed specifications is first designed. Then by replacing analog elements by appropriate digital realizations, the LC ladder filter is transformed into a wave digital filter.

In this way the wave digital filter imitates the behavior of an equally terminated LC ladder filter which is inherently low sensitivity structure. So the wave digital filter can achieve the extremely low sensitivity of attenuation characteristic with respect to coefficient variations.

(2) Roundoff Noise

Consider the roundoff noise generated by a multiplier in a wave digital filter. We examine the wave

digital filter in Fig. 6 under steady state conditions, assuming that it is fed at node 1 by a sinusoidal signal of frequency Wo and complex amplitude X_1. The corresponding output signal at node 2 is Y_2 and the transfer function from node 1 to node 2 is

$$T_{21} = Y_2/X_1 = e^{-\Gamma} \quad , \quad \Gamma = A + jB \tag{5}$$

and

$$X_4 = \alpha Y_3 \tag{6}$$

All complex amplitudes are assumed to correspond to rms values.

The transfer function T_{31}, T_{24} are

$$T_{31} = Y_3/X_1, \quad T_{24} = Y_2/X_4 \tag{7}$$

The sensitivity of T_{21} with respect to α, has been shown to be given by

$$\frac{\partial T_{21}}{\partial \alpha} = T_{31} T_{24} \tag{8}$$

and

$$\frac{\partial \Gamma}{\partial \alpha} = -\frac{1}{T_{21}} \frac{\partial T_{21}}{\partial \alpha} \tag{9}$$

If we assume the multiplier to be realized with fixed-point arithmetic the rounding operation can be taken into account by injecting into node 4 a roundoff noise signal n of power density spectrum N(w), as shown in Fig. 6(b). The resulting output noise power density is

$$N_2(w) = |T_{24}(jw)|^2 N(w) \tag{10}$$

and the corresponding noise-to-signal power ratio is

$$\Phi(w) = N_2(w)/|Y_2|^2 \tag{11}$$

If we now eliminate X_1, Y_2, X_4, T_{21}, T_{31} and $N_2(w)$ among the above expressions (5) - (11) we obtain

$$\Phi(w) = \frac{\Delta^2}{6r^2} \left| \frac{\partial \Gamma(jw)}{\partial \alpha} \right|^2 \cdot \left| \frac{T_{24}(jw)}{T_{24}(jw_0)} \right|^2 \tag{12}$$

where Δ is the quantization step of the signal parameter and r is a positive quantity such that $r < 1$.

For $w = w_0$, (12) reduces to

$$\Phi(w_0) = \frac{\Delta^2}{6r^2} \left| \frac{\partial \Gamma(jw_0)}{\partial \alpha} \right|^2 \tag{13}$$

and then we have

$$\frac{\partial \Gamma(jw_0)}{\partial \alpha} = \frac{\partial A(j\varphi_0)}{\partial \alpha} + j \frac{2\varphi_0}{\pi} \int_0^\infty \frac{\partial A(\varphi)}{\partial \alpha} \cdot \frac{\partial \varphi}{\varphi^2 - \varphi_0^2} \tag{14}$$

where

$$\varphi = \tan(wT/2) \ , \ \varphi_0 = \tan(w_0 T/2)$$

This result shows that the output noise-to-signal ratio depends essentially on the attenuation sensitivity Therefore the wave digital filter with low sensitivity of the attenuation produce less roundoff noise.

4. Experiment and Discussion

A third-order Butterworth digital filter is to be designed as a wave digital filter. Its cutoff frequency is specified as 100Hz with the sampling frequency set at 10KHz.

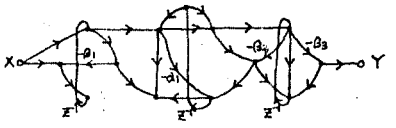

Fig.7 Signal flow graph of the wave digital filter which is designed by the mixed realization

In order to examine the effect of quantization of the nultimplier coefficients in the wave digital filter, the plot of the magnitude characteristic is shown in Fig.8 and to make a comparison the magnitude characteristic of the digital filter implemented in cascade form is also shown in Fig.8.

In Fig.8 we know that the realization is possible down to 10 11 bits for the wave digital filter compared to 16 bits for the cascade.

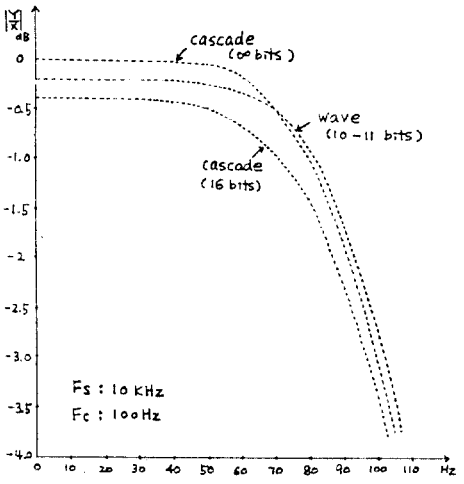

Fig.8 Frequency response of the filter

5. Conclusions

In this paper the design and properties of the wave digital filter which is modeled via transmission-line transformation from analog LC ladder filter was examined.

The outcome of the simulation showed us that the wave digital filter with fixed-point coefficients can be implemented with 5-6 bits shorter coefficient word lengths than the cascade form digital filter with fixed-point coefficients.

Particularly when it is implemented with special-purpose digital hardware the number of registers to store the filter coefficient valves is to be reduced. Therefore the manufacturing costs will be downed.

In a while, because of topological constraints of the wave digital filter the minimum time to process one filter cycle can be longer than the cascade form digital filter.

References

1. A. Fettweis, "Some principles of designing digital filters imitating classical filter structures," IEEE Trans. Circuit Theory (Corresp.), vol. CT-18, pp.314-316, Mar. 1971.
2. A. Fettweis, K. Meerkötter, "On adaptors for wave digital filters," IEEE Trans. Vol. ASSP-23, pp.516-525, Dec. 1975.
3. A. Antoniou, Digital Filters: Analysis and Design. McGraw-Hill, 1979, pp.309-331.
4. R. Levy, "A general equivalent circuit transformation for distributed networks," IEEE Trans. Circuit Theory (Corresp.), Vol. CT-12, pp.457-458, Sept. 1965.
5. A. Fettweis, "On the connection between multiplier word length limitation and roundoff noise in digital filters," IEEE Trans. Circuit Theory, Vol. CT-19, pp.486-491, Sept. 1972.
6. L.B. Jackson, "On the interaction of roundoff noise and dynamic range in digital filters," Bell Syst. Tech. J., Vol. 49, pp. 159-184, Feb. 1970.