Topological analysis of DC motor driving by John's Chopper Circuit

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ABSTRACT :

The purpose of this paper is to develop an efficient model for the analysis of a John's Chopper Circuit.
In the John's Chopper Circuit analysis, the open branches are removed from the associated graph to formulate the modified incidence matrix. An alogorithm for the generation of a modified proper tree and fundamental cut set matrix from a network graph is developed, which utilizes much less computer stroage space and computation time compared to the classical methods.

INTRODUCTION

The chopper controlled DC separately and series excited motors are now widely used in traction and many other industrial applications. In motor DC drives, the classical motor-generator set has been replaced by a thyristorized power convertor which provides faster response at a lower total cost.
In digital computation of thyristors and diodes are replaced by switches and their switchings are determined by their voltages, currents and gate signals.
The "on" switch is represented by a series combination of voltage and a small resistance, while the "off" switch is represented by very large resistence.
Network topology makes use of the formulation of the state equations in the computer.
The purpose of the present paper is to make use of network topology for the formulation of state equations in the thyristor circuits with the main object of eliminating the problem of widely varing time constants and a generalized digital simulation method for the analysis of chopper fed DC motor.
The important features of this method are

1) It can be used for any chopper circuits.

Only the circuit connection and the parameters of circuit elements are needed as the input data.

2) It does not need the prior knowledge of different modes of operation of the chopper circuit and derivation of the relevant equations.

The program itself enables one to determine the node sequence and derive and solve the

system equations automatically.

3) For minimizing computer time in forming the state equations, the "off" switch can be easily removed by Revankar's approach.

4) The Runge-Kutta methods used in this paper are based on fourth-order Taylor approximation.

II. Topological partitioning of the thyristor circuits

It is convenient to partition the fundamental loop and cut-set matrices according to the nature of network elements.
The order of numbering the network branches is E(voltage source), C(capacitance), R(resistance), Switches(SCR, Diode), L(inductance), and J(Current source).
In the graph of the thyristor circuit, all the switching device branches are oriented from anode to cathode to represent the possible current flow direction.

III. Normal Tree

Define a "normal tree" as a having as twigs all of the independent voltage sources, the maximum possible number of capacitors, the minimum possible number of inductors, and none of the independant current sources.

The algorithim for formulation the modified complete incidence matrix is follows:

(a) In the columns of Aa corresponding to the off-switches replace all nonzero entries by zeros.

(b) Check up the rows for one nonzero entry. If such a row exist, then replace its nonzero entry by a zero.

(c) Check the columns for one nonzero entry. If such a column exists, then replace its nonzero entry by a zero.

(d) Repeat steps (b) and (c) till none of the rows and column contain one nonzero entry.

(e) Formulate Aam by eliminating the rows and columns containing all zeros.

$$A = \left(A_t \mid A_l \right)$$

A_t : twig branches matrix
A_l : link branches matrix
A : incidence matrix

IV. Formulation of state equation and elementary propeties

Normal form of the state equation is

$$\frac{dx}{dt} = A_1 X + B_1 U$$

where X is the state vector

U is the input vector

and A_1 and B_1 are the matrices evaluated on basis of cut set submatrix Q_1

V. Switching-device voltage and current relations

On-switching branch current are given by

$$i_{Rt} = -Q_{RR} i_{RL} - Q_{RL} i_{LL} - Q_{Rj} i_j , \qquad V_m = [A_t']^{-1} V_t$$

The fundamental loop matrix B for this choice of normal tree is illustrated in Fig. 4 (b). Where the dashed lines shows the partitioning of the submatrix F.

S : link elastance — C : tree branch capcitances

R : link resistance — G : " " conductances

L : link inductance — F : " " reciprocal inductances

symmetric admittance matrix : $\mathcal{Y}$ — current transfer matrix : $\mathcal{H}$

impedence matrix : $\mathcal{Z}$ — voltage transfer matrix : $-\mathcal{H}'$

VI. Conclusion

The described program can make fast computational time by Revankar's method using the modified incidence matrix obtained by removing "off" switch.

VII. References

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3. Fitzgerald, Kingsley Kusko, Electric machinery, pp 442-448.
4. Franklin KUO, Computer Applications in Electrical Engineering Series. pp 371-395.
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VIII Appendix

$$\mathcal{Y} \equiv F'_{RC} R^{-1} F_{RC}. \qquad \mathcal{H} \equiv F'_{LC} - F'_{RC} R^{-1} F_{RG} R_2 F'_{LG}.$$

$$\mathcal{Z} \equiv F_{LG} S^{-1} F'_{LG}. \qquad -\mathcal{H}' \equiv -F_{LC} + F_{LG} S^{-1} F_{RG} G_1 F_{RC}.$$

$$F = \begin{bmatrix} F_{SC} & 0 & 0 \\ F_{RC} & F_{RG} & 0 \\ F_{LC} & F_{LG} & F_{LF} \end{bmatrix}$$

$$A_1 = \begin{bmatrix} e^{-1} & 0 \\ 0 & \mathcal{L}^{-1} \end{bmatrix} \begin{bmatrix} -\mathcal{Y} & \mathcal{H} \\ -\mathcal{H}' & -\mathcal{Z} \end{bmatrix} = \begin{bmatrix} -e^{-1}\mathcal{Y} & e^{-1}\mathcal{H} \\ -\mathcal{L}^{-1}\mathcal{H}' & -\mathcal{L}^{-1}\mathcal{Z} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} e^{-1} & 0 \\ 0 & \mathcal{L}^{-1} \end{bmatrix} \begin{bmatrix} ' & F'_{RC} R^{-1} F_{RG} R_2 & 0 & F'_{SC} C_1 & F'_{RC} R^{-1} & 0 \\ 0 & -F_{LG} S^{-1} & -F_{LF} L_{22} - L_{12} & 0 & -F_{LG} S^{-1} F_{RG} & I \end{bmatrix}$$

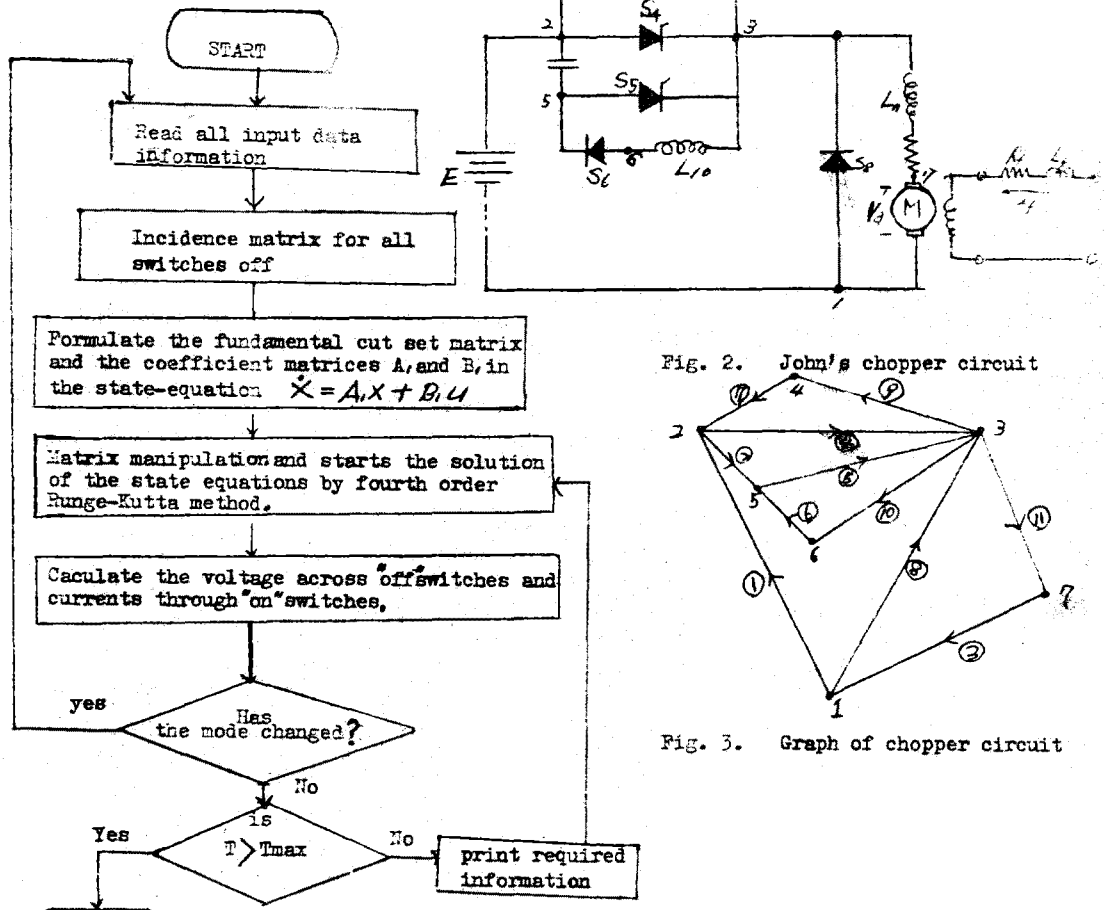

Fig. 1. General flow chart

Fig. 2. John's chopper circuit

Fig. 3. Graph of chopper circuit

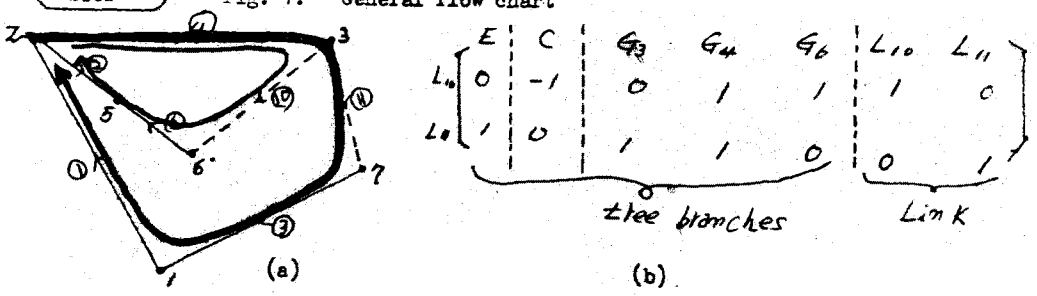

Fig. 4.(a) Normal tree corresponding to off-switch branches 5,7 and 8 .

(b) fundamental loop matrix B.