Fabrication of I^2L by New Process and Its Chracteristics

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Since its introduction in 1972, integrated injection logic(I^2L), or merged transistor logic(MTL), has received the close attentio of LSI researchers, due to its high packing density, excellent spee power product, low fabrication cost, and compatibility with analog circuits.

The basic building block of an I^2L is the single-input multi-output inverter shown schematically in Fig. 1-a. The standard I^2L gate structure, as shown in Fig. 1-b, is fabricated by diffusing two adjacent p-type regions into the n-type wafer, then diffusing n^+-regions into one of the p-type regions. The structure of basic I^2L, as shown in Fig.1-b, is very simple, due to merged transisto structure, and results in few metal interconnections. The collecto is the top n^+-diffused region and the common emitter is the n^+-substrate. The p-regions form the emitter and collector of the pnp transistor.

Initially I^2L circuits were fabricated using standard bipolar diffusion technique and resulted in impressive performance chrac-teristics. However, the standard I^2L structure has some disadvan-tages such as low upward current gain and low speed operation.

A modified npn transistor structure with double base has been proposed to improve the speed and to increase the upward current gain. However, the modified structure requires different doping in the extrinsic base region from the intrinsic region and the complexity of the process is increased[1]. A high performance I^2L process using only five masks was proposed by Seo[2], which is ex-pected to improve the performances of I^2L such as current gain of the pnp and npn transistor and speed power product.

The new fabrication process uses spin-on source as the diffusion source. The I^2L structure using the new process is shown in Fig.2-d. Fig.2 shows the new fabrication process. The fabrication sequen ce is listed below.

1) Diffuse heavily doped n^+ collar on n/n^+ silicon wafer to minimize extraneous base current of the npn transistor.
2) Boron predeposition in the injector and base region. (Fig. 2-a)
3) Arsenosilicafilm coating and photomasking to remove the arsenosilicafilm except collector regions. (Fig.2-b)
4) Borosilicafilm coating.(Fig.2-c)
5) Simultaneous diffusion of boron and arsenic and removing the spin-on sources. Here, the arsenosilicafilm acts as a masking layer against the borosilicafilm during diffusion.
6) Reoxidation,contact and metallization.

I^2L test devices including 13-stage ring oscillator have been fabricated by the new process proposed by Seo. As a starting material, silicon (111) wafers uniformly doped n^+ with a 6.5μm n^- epitaxial layer of concentration $10^{16}cm^{-3}$ have been used.

An upward npn current gain of 8, a speed power product of 3.5 pJ and a minimum propagation delay time of 50ns with standard device breakdowns(BV_{CBO}) of 22 volts have been obtained.

Fig.3 shows the upward current gain versus collector currents of a three collector I^2L gate. Compared with others'(2)(3), improvement in the upward current gain by a factor of 2 is achieved and the upward current gain fall-off of collectors farther away from the base contact due to base resistance at high current range is reduced. And the test results show that the current gain control of the npn transistors can be easily achieved by varying the sheet resistance in the intrinsic base region during boron predeposition step.

References

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(2) K.S.Seo,"A Study on the Integrated Injection Logic-Analysis and New Fabrication Process,"M.S.Thesis of KAIS,1978.
(3) J.L.Saltich,et al,"Processing technology and AC/DC Chracteristics of Linear Compatible I^2L," IEEE J.Solid-State Circuits, Vol.SC-11,Aug.1976.

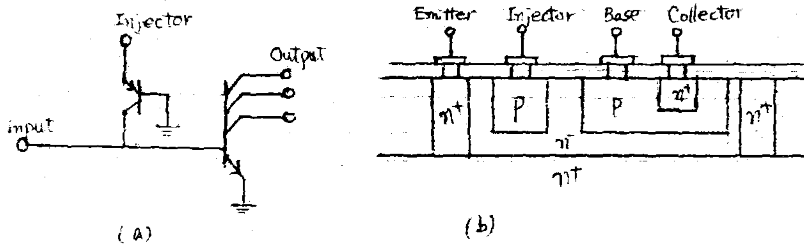
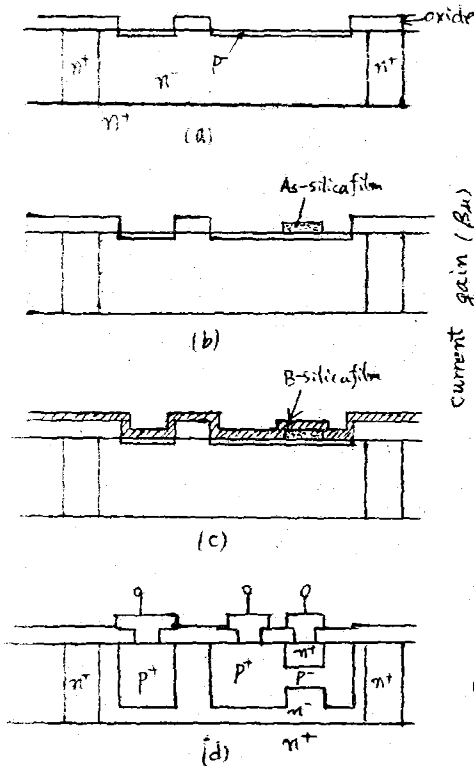


Fig.1. (a) Schematic diagram of an I²L gate
(b) Crosssectianal view of a standard unit cell.



g 2 New process sequence

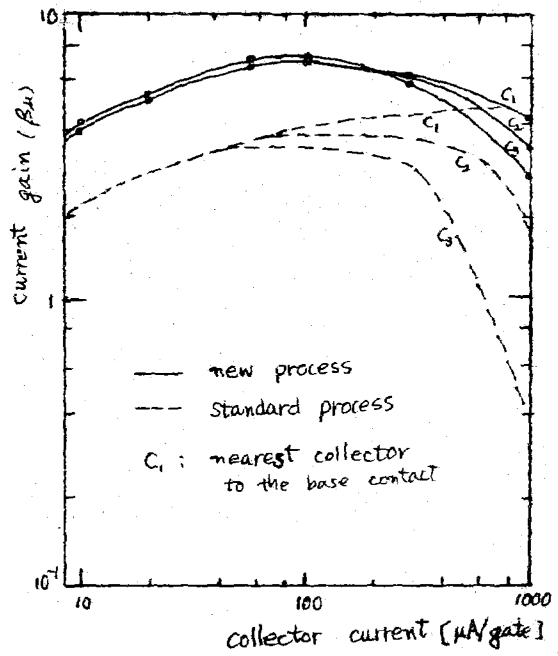


Fig.3 Upward current gain of a three collector I²L. (*: thin epi-wafer)