Three-Phase Current Balancing Strategy with Distributed Static Series Compensators

Hanjong Yoon*, Dongkwan Yoon*, Dongmin Choi*, and Younghoon Cho†

†,*Department of Electrical Engineering, Konkuk University, Seoul, Korea

Abstract

This paper proposes a three-phase current balancing strategy in a power transmission system employing distributed static series compensators (DSSCs). With the proposed variable quadrature voltage injection method, the DSSC emulates either an inductive or a capacitive impedance into the transmission line, and the magnitudes of the phase currents are balanced. Hence, the phase imbalances in the power transmission system are significantly reduced. As a result, the power transfer capability of the transmission lines can be improved. The operational principle of the DSSCs, the hardware structure and the control algorithm are described in detail. Finally, the theoretical analyses and the proposed strategy are experimentally verified through a scaled down transmission system with DSSC prototypes.

Key words: Distributed static series compensator, Power transmission system, Reactive power compensation, Static series compensator

I. INTRODUCTION

A Flexible Alternating Current Transmission System (FACTS) is a static power conditioning system equipped in power transmission systems [1]-[5]. By using FACTS devices, it is possible to feature power flow control, phase imbalance compensation, power quality improvement, and so on. Recently, distributed generation sources have been increasing, which may stimulate the installation of FACTS devices to maximize the utilization of distributed generation sources and transmission lines. Although the advantages of FACTS devices are very useful in practical power transmission systems, their installation is not very popular due to some drawbacks such as a huge initial investment, a bulky volume, complexity in terms of installation, etc. In order to resolve these issues, the concept of distributed FACTS (DFACTS) was introduced [6], [7]. In DFACTS devices, multiple small scaled modules are employed to feature the roles of FACTS devices. One approach is hanging the DFACTS devices to a transmission line and controlling them to adjust its reactance. By doing so, the disadvantages of FACTS devices are significantly mitigated.

Among various FACTS devices, static series compensators (SSCs) are widely used to actively control the reactance of a transmission line, and their DFACTS counterparts are distributed static series compensators (DSSCs) [6], [7].

The concepts of DFACTS and DSSC were introduced in [6]. In that paper, the hardware implementation, control method, and experimental results of the DSSC were described. The authors of [8] verified that DSSCs can improve power system reliability through the investigation of DSSC models. Static synchronous series compensators using daisy-chained transformers were introduced in [9]. The circuit structure and paralleling of the compensators were also studied. An effective deployment of DSSCs was proposed in [10]. In that paper, a linearized transmission system model was introduced, and the simple deployment algorithm was investigated. The authors of [11] discussed the optimal placement of DSSCs while considering the power transfer capability and reliability of the transmission line. A multi-level series compensator was proposed to compensate for voltage sags and swells, harmonics, and reactive power in [12]. Although the effectiveness and the potential performance of DSSCs have been actively studied, their implementation and control have not received a lot of attention.

In this paper, the control structure and hardware design of a DSSC is introduced. The principle of reactive power compensation in a single-phase system is analyzed, and the
key concept of reactive compensation using a DSSC is suggested. To implement this compensation, the variable quadrature voltage injection method is investigated. By using this method, either an inductive or a capacitive impedance is added to the transmission line. Since the reactive component in the line is adjustable, the magnitude and phase of the line current can be regulated. After that, the proposed method is expanded to a three-phase system. The three-phase voltage vector diagram under the unbalanced phase current condition is studied, and approximated voltage vectors to compensate the phase imbalance are obtained with the three-phase quadrature voltage vector injection method. The proposed method is verified through simulation and the experimental results based on a scaled down transmission system with DSSC prototypes. From the obtained simulation and experimental results, it is confirmed that the reactive component in the transmission line can be adjusted, and that the phase current imbalance is significantly compensated with the DSSC.

This paper is organized as follows. The single-phase SSC and its operational principle are introduced in Section II. Section III describes the reactive power compensation with the DSSC in a three-phase system. In addition, the variable quadrature voltage injection method is proposed. Simulation and experimental results are illustrated in Section IV and Section V. Finally, some conclusions are offered in Section VI.

II. SINGLE-PHASE STATIC SERIES COMPENSATORS

A. Principle of Reactive Power Compensation

Fig. 1 illustrates an equivalent circuit model of a transmission line in a power system, where $v_{sx}$ and $v_{rx}$ represent the sending end and receiving end voltages per phase. Here it is assumed that only the inductive line impedance $Z_L$ is existent in the transmission line. The voltage difference $v_x$ between $v_{sx}$ and $v_{rx}$ is defined as:

$$v_x = v_{sx} - v_{rx}$$

(1)

The line current $i_x$ is written as:

$$i_x = \frac{v_x}{Z_L}$$

(2)

By using the phasor expression, $v_x$ and $i_x$ can be rewritten as follows:

$$v_x = |V_x| \angle \theta_x$$

(3)

$$i_x = |I_x| \angle \theta_x$$

(4)

where $\theta_x$, $\theta_s$, $V_x$ and $I_x$ are the phase angles and magnitudes of $v_x$ and $i_x$. By considering a pure inductive impedance, (4) can be rewritten as (5), where the phase of the line current lags the phase of $v_x$ by 90°:

$$i_x = \frac{|V_x|}{X_L} \angle (\theta_x - 90°)$$

(5)

Equation (10) implies that the magnitude of $i_x$ can be adjusted by the states of individual elements. Here, $V_x$ and $X_L$ in (10) cannot be directly controlled since they are dependent on the sending end and receiving end values and the physical configuration of the transmission line. The only opportunity for modification in (10) is $V_q$. Hence, it is possible to adjust $i_x$ as long as $V_q$ can be controlled. This is one of the most important concepts to control the line current with static series compensators. The injected voltage $V_q$ needs to be examined further. As can be seen in (6) and (8), the phase difference between $v_q$ and $i_x$ is either positive or negative 90°. By reflecting this, the injected voltage $v_q$ is called the quadrature voltage [6], [7]. The injected impedances $Z_q$ is defined as:

$$Z_q = \frac{v_q}{i_x} = \frac{|V_q| \angle \theta_q \pm 90°}{|I_x| \angle \theta_x} = \frac{|V_q|}{|I_x|} \angle \pm 90° = \pm jX_q$$

(11)

where $X_L$ is the inductive reactance of the line. A voltage source $v_q$ whose phase is either $90°$ leading or lagging $v_x$ is inserted into the transmission line, as shown in Fig. 2, where the two voltage sources, $v_{sx}$ and $v_{rx}$, are lumped into $v_x$.

If the phase of $v_q$ leads $i_x$ by $90°$, $v_q$ and the difference between $v_x$ and $v_q$ are written as (6) and (7):

$$v_q = |V_q| \angle (\theta_q - 90°) $$

(6)

$$v_x - v_q = (|V_x| + |V_q|) \angle \theta_x$$

(7)

where $V_q$ is the magnitude of $v_q$. On the other hand, the relationships in (8) and (9) are established when $v_q$ lags $i_x$ by $90°$.

$$v_q = |V_q| \angle (\theta_q + 90°) $$

(8)

$$v_x - v_q = (|V_x| - |V_q|) \angle \theta_x$$

(9)

Through equations (5) through (9), the relationships among $i_x$, $V_x$, $V_q$, and $X_L$ is unified as below:

$$i_x = \frac{|V_q|}{X_L} \angle (\theta_x - 90°)$$

(10)

Fig. 1. Equivalent circuit model of a transmission line.

Fig. 2. Transmission line with an additional series voltage source.
where the artificially injected reactance $X_{q}$ by $v_{q}$ is:

$$X_{q} = \frac{v_{q}}{i_{x}}$$

From (11), if $v_{q}$ lags $i_{x}$ by 90°, the polarity of the equivalent reactance becomes negative. As a result, $X_{q}$ works as a capacitive reactance. On the other hand, $X_{q}$ becomes an inductive reactance when $v_{q}$ leads $i_{x}$ by 90°. The total equivalent reactance including $X_{L}$ and $X_{q}$ is written as below.

$$X_{eq} = X_{L} + X_{q}$$

By replacing $X_{eq}$ with $X_{L}$ in (10), $i_{x}$ can be easily adjusted. If $X_{eq}$ is a capacitive reactance, the magnitude of $X_{eq}$ is reduced, and more $i_{x}$ flows through the transmission line. Meanwhile, $X_{eq}$ as an inductive reactance reduces $i_{x}$. This is a very useful property to adapt the SSC to control the power flow, phase balancing, and so on.

**B. Single-Phase Distributed Static Series Compensator**

Fig. 3 represents the fundamental concept of reactive power compensation using DSSCs. Here the multiple quadrature voltages are injected with the multiple DSSCs. By doing so, either the capability of the injected power is increased or the ratings of the individual DSSCs are reduced. The circuit configuration of a single DSSC is shown in Fig. 4. The DSSC consists of a voltage source inverter (VSI), an LC filter and a low frequency transformer, whose number of turns at the primary and secondary sides are $K$ and 1, respectively. In the circuit, the VSI synthesizes the switching waveform, and it is filtered by the LC filter. Then the fundamental component is transferred to the secondary side of the low frequency transformer. Finally, the output voltage $v_{q}$ is produced, and the DSSC can be operated as either a capacitive reactance or an inductive load depending on the phase of $v_{q}$.

At the dc side of the VSI, only a dc-link capacitor is equipped, and the DSSC receives active power from the transmission line to charge the dc-link voltage. It should be noticed that the DSSC only compensates reactive power, since it does not contain an active power source. In fact, dc-link voltage supplied from the transmission line is used to compensate the reactive power in the transmission line.

Fig. 5 represents a control block diagram of the proposed DSSC which consists of a dc-link voltage controller, a single-phase phase-locked-loop (PLL), and a reference generator for the phase angle. The single-phase PLL takes the line current as its input, and the phase angle of the line current $\theta_{c}$ is estimated. Since $\theta_{c}$ is the reference angle of the entire compensation, the accuracy of the single-phase PLL is critical in the control block. In this paper, the orthogonal signal generation based PLL described in [13] is utilized. The reference generator block commands the polarity of the compensation angle $\theta'$ whose magnitude is fixed to 90°. If the DSSC needs to be operated in an inductive reactance mode, the polarity of $\theta'$ is positive. If a capacitive reactance is necessary, the polarity of $\theta'$ is negative. The dc-link voltage controller consists of a proportional-integral (PI) controller to regulate the dc-link voltage according to the reference voltage. In the proposed method, the modulation index of the DSSC inverter is fixed to a certain value, which is close to the unity value, since such a high modulation index can reduce the current ripple. As a result, the size of the magnetic components can be effectively reduced. It means that the peak magnitude of $v_{q}$ is mainly determined by the dc-link voltage. Accordingly, the performance of the dc-link voltage controller directly affects the dynamic property of the compensation via the DSSC. In order to regulate the dc-link voltage, a certain amount of active power is necessary due to the parasitic in the circuit. The output of the dc-link voltage controller is the phase angle $\theta_{c}$ of the active power transfer. In sum, the phase angle of $v_{q}$ is calculated as follows:

$$\theta_{c} = \theta_{c} + \theta' + \theta_{r}$$

In addition, the injected voltage $v_{q}$ is finally obtained as:

$$v_{q} = MV_{dc} \sin(\theta_{c})$$
Fig. 6. Simulation results for a single-phase DSSC in the capacitive and reactive reactance injection modes. (a) Line current. (b) dc-link voltage and quadrature voltage. (c) Delivered real and reactive power. (d) Injected real and reactive power by the DSSC.

The apparent power that is injected by the DSSC is represented as follows:

\[ S_x = v_{qs}^* i_s^* \]  \hspace{1cm} (16)

where \( i_s^* \) is the complex conjugate of the line current \( i_s \). At the steady state, \( v_{qs} \) and \( i_s^* \) are written as follows:

\[ v_{qs} = M V_{dc} \angle \theta_{ds} \pm 90^\circ \]  \hspace{1cm} (17)

\[ i_s^* = i_s \angle -\theta_{ds} \]  \hspace{1cm} (18)

By substituting (17) and (18) into (16), \( S_x \) is simplified as:

\[ S_x = M V_{dc} i_s \angle \pm 90^\circ = j Q_x \]  \hspace{1cm} (19)

where \( Q_x \) is defined as:

\[ Q_x = M V_{dc} i_s \]  \hspace{1cm} (20)

Equation (19) implies that the DSSC only injects reactive power. This is due to the fact that no active dc source is connected to the DSSC. However, parasitics may induce an active power component.

C. Simulation of a Single-Phase DSSC

The operation of a single-phase DSSC is verified through simulations before expanding the compensation concept with DSSCs to three-phase systems. The circuit structure shown in Fig. 4 is analyzed using the PSIM software package. In the simulations, \( v_{ac} \) is implemented as a single-phase ac voltage source whose root-mean-square (RMS) value is 220V. The line impedance \( X_L \) is configured to be 24.95Ω. For the sake of simplicity, the receiving end is assumed to be a resistive load with 50Ω. The parameters of the DSSC are summarized in Table I.

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>PARAMETERS OF THE DSSC</th>
</tr>
</thead>
<tbody>
<tr>
<td>The dc-link capacitance (( C_{dc} ))</td>
<td>1000 ( \mu )F</td>
</tr>
<tr>
<td>The filter inductance (( L_f ))</td>
<td>2 mH</td>
</tr>
<tr>
<td>The filter capacitance (( C_f ))</td>
<td>20 ( \mu )F</td>
</tr>
<tr>
<td>Primary side turns ratio (( K ))</td>
<td>1</td>
</tr>
</tbody>
</table>

Fig. 6 shows simulation results under the capacitive and inductive reactance injection modes for a single-phase DSSC. The simulations are executed for 2 seconds. At \( t = 0.5s \), the dc-link voltage reference \( V_{dc}^* \) is changed from 0V to 75V. Then the DSSC injects the corresponding reactive power. Fig. 6(a) illustrates the line current \( i_s \) and its average peak for different reactance injection modes.
Three-Phase Current Balancing Strategy with DSSC

III. REACTIVE POWER COMPENSATION WITH DSSC IN THREE-PHASE SYSTEMS

A. Analysis of the Phase Current Imbalance

Fig. 8 shows a three-phase transmission line with DSSCs. \( v_{xs} \) and \( v_{xc} \) are the sending and receiving end voltages for phase \( x \) where \( x \) can be \( a, b, \) or \( c \). Similarly, \( v_{qs} \) represent the total quadrature voltages injected by the DSSCs in each phase. The line impedances are represented as \( Z_a, Z_b \), and \( Z_c \). From this figure, the line current \( i_s \) is written as (21).

\[
i_s = \frac{v_{xs} - v_{qs} - v_{rx}}{Z_s} \tag{21}\]

In fact, the receiving end voltages can be replaced with load impedances by assuming there are no generation sources at the points. Then (21) can be rewritten as:

\[
i_s = \frac{v_{xs} - v_{qs}}{Z_x + Z_{load}} \tag{22}\]

where \( Z_{load} \) is the load impedance at the receiving ends. It is assumed that the sending end voltages are balanced. If \( v_{qs} \) is not considered, an unbalanced phase current in the power system can be produced by assuming the existence of mismatch among \( Z_x, Z_{load} \) and \( v_{rx} \). In fact, it is reasonable that there is no voltage imbalance at the receiving end with \( v_{rx} \). This is due to the fact that they are normally established by the generation source. In addition, it can be assumed that the load impedance is balanced since an unbalanced load can be lumped into \( Z_x \). From this, it is possible to simplify the phase current imbalance since it is only caused by the unequal line impedances, \( Z_a, Z_b \) and \( Z_c \). Accordingly, an unbalanced three-phase current is caused by unequal voltage drops in unequal line impedances. On the other hand, the three-phase current can be balanced as long as the voltage drops at individual line impedances are equal.

Fig. 9 shows vector diagrams of the three-phase voltages. In this figure, \( v_{xa}, v_{xb} \) and \( v_{xc} \) are the vectors of the voltage drop at \( Z_a, Z_b \) and \( Z_c \), when they are perfectly balanced. Here \( v_{xa}, v_{xb} \) and \( v_{xc} \) represent the vectors of the voltage drop when there is an impedance imbalance. As explained above, unbalanced load impedances are lumped into the line impedances. As a result, the phase angle differences among individual phases can be different rather than fixed to 120°. To obtain a balanced phase current, \( v_{xa}, v_{xb} \) and \( v_{xc} \) should be rearranged as \( v_{xa}^*, v_{xb}^* \) and \( v_{xc}^* \) by injecting the compensation voltage vectors \( v_{pa}, v_{pb} \) and \( v_{pc} \) with the DSSCs. Then \( v_{pa}, v_{pb} \) and \( v_{pc} \) are obtained as follows:

\[
v_{qs} = v_{xs} - v_{xs} = \left| v_{qs} \right| \sin \left( \omega t + \theta_{vqs} \right), \quad x \in \{a, b, c\} \tag{23}\]
where \( \omega \), \( V_{qs} \) and \( \theta_{qs} \) are the electrical angular velocity, the magnitude of \( V_{qs} \) in phase \( x \), and the phase angle of \( V_{qs} \). In (23), \( V_{qs} \) can be easily adjusted with the DSSCs since it is directly proportional to the modulation index of the VSI and the dc-link voltage. However, there is a limitation to implementing \( \theta_{qs} \) due to the fact that there are no active power sources in the DSSCs. As analyzed above, the phase angle of the DSSC should always lead or lag the phase current by 90°. As a result, “ideal compensation” with the whole modification of both the magnitude and the phase angle of the voltage vector is almost impossible with DSSCs. From now on, \( V_{qa} \), \( V_{qb} \) and \( V_{qc} \) are denoted as ideal compensation vectors, which may not be perfectly synthesized.

**B. Proposed Variable Quadrature Voltage Injection Method**

Since the VSIs in DSSCs cannot produce ideal compensation vectors, it is important to find approximated compensation vectors whose voltage and phase are similar to the ideal compensation vectors. Fig. 10 shows a voltage vector diagram with the proposed algorithm. Unlike the quadrature voltage vector shown in Fig. 9 where the phase of the quadrature voltage can be selected without any restrictions, it is either 90° lag or lead in practical situations. This is due to the fact that there is no energy source to supply active power. In this figure, \( V_{zx}^* \) is the ideal compensation vector, and the capacitive mode is selected. Since the magnitude of \( V_{zx} \) and the phase of \( V_{qs} \) are fixed, \( V_{zx}^* \) cannot be synthesized. Alternatively, a modified compensation vector \( V_{zm}^* \) is selected whose magnitude is close to that of \( V_{zx}^* \). In order to take this into consideration, (23) is modified as follows:

\[
V_{qs} = M_x V_{qs} \sin (\omega t + \theta_{qs} \pm 90°) \quad (24)
\]

where \( M_x \) is the modification factor. By adjusting \( M_x \), a variety of compensation vectors can be alternatively selected, and a three-phase current balance is achieved.

In this paper, this scheme is called the variable quadrature voltage injection (VQVI) method. The key point of VQVI is determining \( M_x \), which maximizes the current balancing capability in three-phase systems. Under this condition, the dc-link voltage reference of phase \( x \) is chosen as (25).

\[
V_{dc,x}^* = M_x V_{qs} \quad (25)
\]

Fig. 11 represents \( M_x \) as a block diagram, and the magnification of the VQVI method \( M_x \) is expressed as:

\[
M_x = M_s + (SGN_x \times \frac{i_{err}}{i_{avg}}) \quad (26)
\]

\( M_s \) is consisted of an operation mode of the DSSC \( SGN_x \), the current error \( i_{err} \) and the average of the peak values of the three-phase line current \( i_{avg} \). When the peak values of the line current in each phase are \( |i_a|, |i_b| \) and \( |i_c| \), the value of \( i_{avg} \) can be calculated as in (27).

\[
\text{avg a b c} i_i = \frac{|i_a| + |i_b| + |i_c|}{3} \quad (27)
\]

In addition, the difference between \( i_{avg} \) and the peak value of the line current in each phase \( |i| \) is defined as the current error \( i_{err} \), which is shown in (28).

\[
i_{err} = i_{avg} - |i| \quad (28)
\]

Thus, the ratio of \( i_{avg} \) and \( i_{err} \) is positive, if \( |i| \) is less than \( i_{avg} \) in (26). However, the ratio of \( i_{avg} \) and \( i_{err} \) is negative, if the phase current \( |i| \) is larger than \( i_{avg} \). The ratio of \( i_{avg} \) and \( i_{err} \) is a fundamental variation of \( M_x \). In addition, the more the magnitude of the phase current is larger than the average value, the more abruptly \( M_x \) changes. However, if the operation mode of the DSSC is different, the change of the line current is also different depending on \( M_x \). When \( M_x \) becomes larger, the line current decreases in the inductor.
mode. However, the line current increases in the capacitor mode. The inductor mode is the current reduction compensation mode, and the capacitor mode is the current increase compensation mode. Thus, $SGN_i$, which represents an operation mode of the DSSC, is used to change the sign of $M_i$ according to the operation mode of the DSSC. $SGN_i$ becomes ‘-1’ in the inductor mode, and $SGN_i$ becomes ‘+1’ in the capacitor mode.

$M_i$ is calculated by the VQVI method for every period. However, when the magnitude of the line current $i$, reaches $i_{avg}$, the value of $M_i$ is not calculated and holds its latest value. To do this, the conditional expression is defined as (29),

$$i_{err} \geq i_{err\_limit}$$

(29)

If the current error $i_{err}$ becomes less than the tolerance $i_{err\_limit}$, the DSSC regulates dc-link voltage determined by $k_c$. If the three-phase line currents reach this condition, the peak value of the line current converges to $i_{avg}$ in each phase. The tolerance $i_{err\_limit}$ is the product of the tolerance $T_{err}(\%)$ and $i_{avg}$. In addition, $i_{err\_limit}$ can be defined as:

$$i_{err\_limit} = i_{avg} \times T_{err}(\%)$$

(30)

When the VQVI method is applied, the three-phase line currents become balanced. However, there is a difference depending on the operation mode of the DSSC in each phase. This operation mode can be set by the user. However, there are a number of cases. DSSCs should have the same the operation mode for all of the phases. In all of the inductor modes, the three-phase line currents are balanced based on the phase with the lowest peak value. Conversely, in all of the capacitor modes, the line current is balanced based on the phase with the highest peak value. However, compensation may not work well in the capacitor mode. In the capacitor mode, if the reactive power absorbed by the DSSC becomes larger than a certain level, the active power is reduced and the line current is decreased. Thus, the user must select a suitable operation mode for the DSSC for better compensation according to the differences between the line current magnitude of each phase.

IV. SIMULATION

The effectiveness of the proposed algorithm is verified through simulations using PSIM software. Fig. 12 shows a system diagram used in both the simulations and the experimentations. The variables in regards to the system parameters and algorithms are defined in the appendix. The DSSC modules are replaced by dependent voltage sources in the simulation for the sake of convenience. These dependent voltage sources apply the quadrature voltage in (10). However, they do not control the dc-link voltage. Thus, they inject pure reactive power (THD=0%) since they are not inverter output voltage. The simulation took 3.2 seconds in total and the operation mode was changed in units of 0.8 seconds as follows:

0–0.8 seconds: No compensation (Quadrature voltage = 0V).
0.8–1.6 seconds: VQVI algorithm (Capacitor mode).
1.6–2.4 seconds: No compensation (Quadrature voltage = 0V).
2.4–3.2 seconds: VQVI algorithm (Inductor mode).

At 0 to 0.8 seconds and 1.6 to 2.4 seconds, the VQVI algorithm is not applied. During these periods, there is no compensation since the DSSC does not inject quadrature voltage. At 0.8 to 1.6 seconds and 2.4 to 3.2 seconds, the VQVI algorithm is applied and the line currents become balanced.

Fig. 13 shows variations of the current maximum values, and Fig. 14 shows the $M_i$ variations of each phase. At 0 to 0.8 seconds and 1.6 to 2.4 seconds, the maximum magnitudes of the three-phase currents are different due to imbalance. In addition, the $M_i$ values of each phase are determined in those periods. The maximum value of the current reference is determined to make the three-phase current balanced, while the phase currents of the A and B phases increase from 0.8 to 1.6 seconds in the capacitor operation mode. In addition, the maximum current references of the A and B phase are based on the largest C phase. This is due to the fact that it does not need to increase the current of the C phase and the value of
Fig. 15. Simulation results of the line current in the VQVI algorithm. (a) No compensation. (b) Compensation: capacitor mode. (c) Compensation: inductor mode.

Fig. 16. Simulation results of the receiving-end voltage in the VQVI algorithm. (a) No compensation. (b) Compensation: capacitor mode. (c) Compensation: inductor mode.

Fig. 17. Simulation results of $v_{sa}$, $v_{sb}$, $v_{qsa}$ and $i_b$ of phase B in the VQVI algorithm. (a) No compensation. (b) Compensation: capacitor mode. (c) Compensation: inductor mode.

$M_e$ becomes 0. Fig. 15 to Fig. 17 show waveforms when three-phase DSSCs operate in the inductor mode and the VQVI algorithm is applied. When operating in the inductor mode, the magnitude of the phase A and phase B currents decrease to that of the three-phase balance. In addition, the receiving-ends voltage also decreases.

Fig. 15 and Fig. 16 represent the line current and receiving-ends voltage. In addition, Fig. 17 represents the receiving end voltage, sending end voltage, line current, and quadrature voltage. When operating in the capacitor mode, the magnitude of the phase A and B currents increases to that of three-phase balanced. In addition, the receiving-ends voltage also increases.

V. EXPERIMENTS

Experiments were implemented to demonstrate the proposed algorithm. The configuration of the system in experiments is the same as that shown in Fig. 21. There are a VariAC that modifies the input voltage, a high voltage transmission line model scaled down to 1/1000, DSSC modules, and a series resistor and inductor for the line impedance model. Experiments were conducted in different operation modes for 120 seconds. From 0 to 30 seconds, there is no compensation. Therefore, the quadrature voltage is 0V. From 30 to 60 seconds, the VQVI algorithm operates in the capacitor mode. From 60 to 90 seconds, there is no compensation. From 90 to
Three-Phase Current Balancing Strategy with …

Fig. 18. Experiment results of the line current in the VQVI algorithm. (a) No compensation. (b) Compensation: capacitor mode. (c) Compensation: inductor mode.

Fig. 19. Experimental results of the receiving-end voltage in the VQVI algorithm. (a) No compensation. (b) Compensation: capacitor mode. (c) Compensation: inductor mode.

Fig. 20. Experimental results of \( v_{sb}, v_{rh}, v_{qb}, \) and \( i_b \) of phase B in the VQVI algorithm. (a) No compensation. (b) Compensation: capacitor mode. (c) Compensation: inductor mode.

Although the compensation algorithm is not applied, Fig. 20(a) shows that the quadrature voltage of phase B is not 0 unlike Fig. 17(a). This is due to the fact that there is an active power compensation to maintain the dc-link of the DSSC modules in actual experiments. For this reason, the quadrature voltage \( v_{qb} \) contains harmonics as shown in Fig. 20(b) and 20(c).

Table III shows the results obtained from the experiments. This table shows the peak current values \( I_{x, \text{peak}} \), phase differences, and algorithm scale values \( M_x \) for each of the lines. After applying the VQVI algorithm, the magnitude of the error and the phase difference become smaller as in the simulation. However, in the experimental result, the error is larger than that in the simulation. This difference between the experiment and the simulation is caused by the way the compensation voltage is supplied. In the simulation, a dependent voltage source is used to supply the compensation voltage instead of an inverter. On the other hand, in the
TABLE II
SIMULATION RESULTS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NO Compensation</th>
<th>Capacitor Mode</th>
<th>Inductor Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>$i_a_{peak}$</td>
<td>5.09A</td>
<td>5.477A</td>
<td>5.063A</td>
</tr>
<tr>
<td>$i_b_{peak}$</td>
<td>5.24A</td>
<td>5.477A</td>
<td>5.063A</td>
</tr>
<tr>
<td>$i_c_{peak}$</td>
<td>5.48A</td>
<td>5.479A</td>
<td>5.065A</td>
</tr>
<tr>
<td>Phase(A-B)</td>
<td>117.47°</td>
<td>119.97°</td>
<td>119.97°</td>
</tr>
<tr>
<td>Phase(A-C)</td>
<td>233.08°</td>
<td>239.95°</td>
<td>239.97°</td>
</tr>
<tr>
<td>$M_a$</td>
<td>0.0</td>
<td>2.052</td>
<td>0.126</td>
</tr>
<tr>
<td>$M_b$</td>
<td>0.0</td>
<td>1.264</td>
<td>0.85</td>
</tr>
<tr>
<td>$M_c$</td>
<td>0.0</td>
<td>0.0</td>
<td>2.024</td>
</tr>
</tbody>
</table>

Fig. 21. Experimental setup.

TABLE III
EXPERIMENT RESULTS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NO Compensation</th>
<th>Capacitor Mode</th>
<th>Inductor Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>$i_a_{peak}$</td>
<td>5.11A</td>
<td>5.51A</td>
<td>5.06A</td>
</tr>
<tr>
<td>$i_b_{peak}$</td>
<td>5.26A</td>
<td>5.53A</td>
<td>5.05A</td>
</tr>
<tr>
<td>$i_c_{peak}$</td>
<td>5.50A</td>
<td>5.54A</td>
<td>5.09A</td>
</tr>
<tr>
<td>Phase(A-B)</td>
<td>116.01°</td>
<td>121.63°</td>
<td>119.72°</td>
</tr>
<tr>
<td>Phase(A-C)</td>
<td>227.38°</td>
<td>242.64°</td>
<td>238.27°</td>
</tr>
<tr>
<td>$M_a$</td>
<td>0.0</td>
<td>3.782</td>
<td>0.0</td>
</tr>
<tr>
<td>$M_b$</td>
<td>0.0</td>
<td>2.843</td>
<td>0.94</td>
</tr>
<tr>
<td>$M_c$</td>
<td>0.0</td>
<td>0.0</td>
<td>2.988</td>
</tr>
</tbody>
</table>

Fig. 22. Experiment results for variations of $|i_a|$, $|i_b|$ and $|i_c|$.

Fig. 23. Experiment results for variations of $M_a$, $M_b$ and $M_c$.

The peak value of line current (A)
Time (s)

The magnitude of the line current (A)
Time (s)

experiment, an inverter is used to supply the compensation voltage. Thus, there are output voltage harmonics that make the error increase.

Fig. 22 and Fig. 23 show the variation of peak current and $M_i$ of each phase in the experiment. In addition, the value of $M_i$ is increased up to 1.8 times higher than the simulation results. As a result, the experiment has an error in the current measurement and a sampling delay. The VQVI algorithm includes an integral term, which can affect the current measurement error and time delay. In addition, the maximum value of the current in Fig. 22 decreases over time. This is due to the temperature of the winding resistor when the load is increased.

The temperature of the load resistor is over 200 degrees. Therefore, the resistance of the load is increased and the magnitude of the line current is decreased. The experimental results verify the proposed VQVI algorithm proposed in this paper.

VI. CONCLUSIONS

This paper proposed an algorithm to solve the imbalance of three phase line current due to an imbalanced impedance. This is accomplished by using a DSSC which is a reactive power compensator. The proposed algorithm varies the magnitude of the quadrature voltage injected by the DSSC. As a result, the maximum value of the line current of each phase reaches the average value based on the line current. When a variable quadrature voltage is injected into a line, the maximum value of the three-phase current converges to the average value, and the line current forms a balanced three-phase balance. In addition, the effectiveness of the algorithm proposed in this paper is verified with simulation and experimental results. The algorithm proposed in this paper is able to mitigate the imbalance of three-phase current as a reactive power compensator without an external power supply of the transmission system.

APPENDIX

System parameter:

$R_{line\_a} = 1.5\Omega, R_{line\_b} = 1.5\Omega, R_{line\_c} = 1.5\Omega$

$L_{line\_a} = 88.16\text{mH}, L_{line\_b} = 79.82\text{mH}, L_{line\_c} = 66.18\text{mH}$
R_{\text{load}_a} = 1.5\Omega, R_{\text{load}_b} = 1.5\Omega, R_{\text{load}_c} = 1.5\Omega
L_{\text{load}_a} = 4.128\text{mH}, L_{\text{load}_b} = 4.128\text{mH}, L_{\text{load}_c} = 4.128\text{mH}
\nu_{sa} = 311\sin(377t+120^\circ)V, \nu_{sb}= 311\sin(377t)V, \nu_{sc} = 311\sin(377t-120^\circ)V
C_{dc} = 1000\mu\text{F}, C_f = 20\mu\text{F}, L_f = 2\text{mH}

ACKNOWLEDGMENT

This work was supported by “Human Resources Program in Energy Technology” of the Korea Institute of Energy Technology Evaluation and Planning (KETEP), granted financial resource from the Ministry of Trade, Industry & Energy, Republic of Korea. (No. 20174030201660)
This research was supported by Korea Electric Power Corporation through Korea Electrical Engineering & Science Research Institute. [Grant number: R15XA03-34]

REFERENCES


Hanjong Yoon was born in Seoul, Korea, in 1991. He received his B.S. degree in Electrical Engineering from Konkuk University, Seoul, Korea, in 2016, where he is presently working towards his Ph.D. degree. His current research interests include the power electronics converters in power system applications.

Dongkwan Yoon was born in Seoul, Korea, in 1991. He received his B.S. degree in Electrical Engineering from Konkuk University, Seoul, Korea, in 2017, where he is presently working towards his Ph.D. degree. His current research interests include the power electronics converters in power system applications.

Dongmin Choi was born in Seoul, Korea, in 1992. He received his B.S. degree in Electrical Engineering from Konkuk University, Seoul, Korea, in 2017, where he is presently working towards his Ph.D. degree. His current research interests include grid-tied inverters with WBG devices and on-board chargers.
Younghoon Cho was born in Seoul, Korea, in 1980. He received his B.S. degree in Electrical Engineering from Konkuk University, Seoul, Korea, in 2002; his M.S. degree in Electrical Engineering from Seoul National University, Seoul, Korea, in 2004; and his Ph.D. degree from the Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, in 2012. From 2004 to 2009, he was an Assistant Research Engineer at the Hyundai MOBIS R&D Center, Yongin, Korea. Since 2013, he has been with the Department of Electrical Engineering, Konkuk University. His current research interests include digital control techniques for the power electronic converters in vehicle and grid applications, multilevel converters, and high-performance motor drives.